CCFC2002BC
Data Sheet
Rev 0.1

HCMOS
Microcontroller Unit

IP Design Group
C*Core R&D Center.

Revision History

Release Number	Date	Author	Summary of Changes
0.1	2014.11.11		The original version.

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Section 1 Introduction

1.1 Introduction

CCFC2002BC is a chip based on C2002 PowerPC processor. The process is TSMC0.18 HDR. C2002 processor core is a single-issue, 4-pipeline, PowerPC processor which implements Power Architecture Book E programmer's model and VLE enhancements. CCFC2002BC is targeted to automotive-focused products.
CCFC2002BC uses one C2002 core and high-speed interconnect technolgy(AHB mixed matrix) to balance processor performance with I/O system throughput.
CCFC2002BC has a internal SRAM memory controller, a internal FLASH controller for data and another FLASH controller for code, six flexCAN controller according to the CAN 2.0B protocol specification, two eMIOS controller to detect and measure the timing events, four LINFlex controller, one I2C controller, three DSPI controller, one ADC and the other miscellaneous periperals.
CCFC2002BC is designed for dynamic power management of core and peripherals. Software can controll the clock gating of peripherals. In standby mode, the power supply to the most of peripherals can be switched off for ultra low power consumption.

1.2 Key Features

The following lists an overview of CCFC2002BC key feature set:

- Operation Parameters
  - Up to 64MHz operation frequency
  - –40 °C to 125 °C junction temperature operating range
- C2002 Cores
  - Single-issue, 4-pipeline PowerPC processor
  - 32-bit Power Architecture Book E programmer's model
  - Variable Length Encoding Enhancements
  - Separate instruction bus and load/store bus
  - Memory management unit with 16-entry TLB
  - Vectored interrupt support
  - Non-maskable interrupt(NMI) input for handling emergent external events

  - Scalar single precision FPU
- AHB Bus Controller
  - master ports
  - slave ports
  - 32-bit address, 64-bit data paths
  - Fully concurrent transfers between independent master and slave ports
  - Fixed priority scheme and fixed parking strategy
  - Force round_robin mode
- eFLASH controller
  - 128bits High read parallelism
  - SEC/DED
  - 64bits double word program
  - Sector erase
  - No support for read while write
  - Erase suspend
  - Software programmable program/erase/protection to avoid unwanted writings
  - Censored Mode against piracy
  - Shadow Sector Available for CFLASH
  - One-Time Programmable (OTP) area in Test Flash Block
  - 6 Boot sectors for CFLASH
- Internal SRAM Bus Controller
  - Byte, halfword and word addressable
  - ECC (error correction code) protected with single-bit correction and double-bit detection
  - Divided into three power domain
- MPU
  - Support for 8 memory region descriptors, each 128 bits in size
  - granularity for region sizes from 32 bytes to 4 GB
  - Access control definitions
  - Automatic hardware maintenance of the region descriptor
  - Alternate memory view of the access control word

  - For overlapping region descriptors, priority is given to permission granting over access
  - Support for 4 XBAR slave port connections MPU hardware continuously monitors every XBAR slave port access using the preprogrammed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device.
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes and "detail" information
  - Global MPU enable/disable control bit provides a mechanism to easily load region descriptors during system startup or allow complete access rights during debug with the module disabled
- BAM
  - Manages the serial download (FlexCAN or LINFlex protocols supported) including support for a serial password if censorship is enabled
  - Places the microcontroller into static mode if flash memory boot mode is selected and a valid BOOT_ID is not located in one of the boot sectors by the SSCM
  - System Configuration and Status
  - Memory sizes/status
  - Microcontroller Mode and Security Status
  - Search Code Flash for bootable sector
  - Determine boot vector
  - Device identification information
  - Debug Status Port enable and selection
  - Bus and peripheral abort enable/disable
- DSPI x 3
  - Full-duplex, three-wire synchronous transfers
  - Master and slave mode
  - Buffered transmit and receive operation using the TX and RX FIFOs, with depths of four entries
  - Visibility into TX and RX FIFOs for ease of debugging
  - FIFO bypass mode for low-latency updates to SPI queues
  - Programmable transfer attributes on a per-frame basis
  - Up to 6 peripheral chip selects, expandable to 64 with external demultiplexer

- Deglitching support for up to 32 peripheral chip selects with external demultiplexer
- 6 interrupt conditions:
- Modified SPI transfer formats for communication with slower peripheral devices
- Supports all functional modes from QSPI subblock of QSMCM
- Continuous serial communications clock (SCK)

• ADC

- 10-bit resolution
- 36 channels (depending on package type), expandable to 64 channels via external multiplexing
  - As many as 16 precision channels
  - As many as 20 standard channels, 4 being expandable to as many as 32 external channels
- Address decoder signal generation (alternate functions MA[2:0]) to control external multiplexers
- Individual conversion registers for each channel (internal and external)
- 3 different sampling and conversion time registers CTR[0:2] (internal precision channels, standard channels, external channels)
- As many as 64 data registers for storing converted data. Conversion information, such as mode of
- operation (normal, injected or CTU), is associated to data value.
- Conversion triggering sources:
  - Software
  - CTU
  - PIT channel 2 (for injected conversion)
- 4 analog watchdogs
  - Interrupt capability
  - Allow continuous hardware monitoring of 4 analog input channels
- Presampling (VSS and VDD)
- Conversions on external channels managed in the same way as internal channels, making it
- transparent to the application
- One Shot/Scan Modes
- Chain Injection Mode
- Power-down mode

  - 2 different Abort functions allow to abort either single-channel conversion or chain conversion
  - Auto-clock-off
- INTC
  - Supports 134 peripheral and 8 software-configurable interrupt request sources
  - Unique 9-bit vector per interrupt source
  - Each interrupt source can be programmed to one of 16 priorities
  - Preemption
  - Low latency - 3 clocks from receipt of interrupt request from peripheral to interrupt request to processor
- LINFlex x 4
  - Supports LIN protocol versions 1.3, 2.0, 2.1 and J2602
  - Master mode with autonomous message handling
  - Classic and enhanced checksum calculation and check
  - Single 8-byte buffer for transmission/reception
  - Extended frame mode for In-Application Programming (IAP) purposes
  - Wake-up event on dominant bit detection
  - True LIN field state machine
  - Advanced LIN error detection
  - Header, response and frame timeout
  - Slave mode1
  - Autonomous header handling
  - Autonomous transmit/receive data handling
  - LIN automatic resynchronization, allowing operation with 16 MHz fast internal RC oscillator as clock source
  - 16 identifier filters for autonomous message handling in Slave mode1
- SIUL x 1
  - GPIO
  - External interrupts
  - System configuration
- FlexCANx6

  - Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0-8 bytes data length
  - Programmable bit rate up to 1 Mbit/s
  - Content-related addressing
  - Flexible Message Buffers (up to 64) of zero to eight bytes data length
  - Each MB configurable as Rx or Tx, all supporting standard and extended messages
  - Individual Rx Mask Registers per Message Buffer
  - Includes either 1056 bytes (64 MBs) of SRAM used for MB storage
  - Includes either 256 bytes (64 MBs) of SRAM used for individual Rx Mask Registers
  - Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16
  - standard or 32 partial (8 bits) IDs, with individual masking capability
  - Selectable backwards compatibility with previous FlexCAN version
  - Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
  - Unused MB and Rx Mask Register space can be used as general purpose SRAM space
  - Listen-only mode capability
  - Programmable loop-back mode supporting self-test operation
  - Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
  - Time Stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
  - Independent of the transmission medium (an external transceiver is assumed)
  - Short latency time due to an arbitration scheme for high-priority messages
  - Low power mode
- IIC x1
  - Compliant with Philips Semiconductors I2C Specification, dated 1995

  - APB Interface
  - Two independent 4 x 1 byte data buffers
  - Programmable error recovery
  - Detects illegal start and stop signals
- eMIOS x2
  - 2 eMIOS blocks with 28 channels each
  - One global prescaler
  - 16-bit data registers
  - 10 x 16-bit wide counter buses
  - Control and Status bits grouped in a single register
  - Shadow FLAG register
  - State of the UC can be frozen for debug purposes
  - Motor control capability
- CGM
  - Generates system and peripheral clocks
  - Selects and enables/disables the system clock supply from system clock sources according to MC_ME control
  - Contains a set of registers to control clock dividers for divided clock generation
  - Supports multiple clock sources and maps their address spaces to its memory map
  - Generates an output clock
  - Guarantees glitch-less clock transitions when changing the system clock selection
  - Supports 8-, 16- and 32-bit wide read/write accesses
- RGM
  - 'destructive' resets management
  - 'functional' resets management
  - signalling of reset events after each reset sequence (reset status flags)
  - conversion of reset events to SAFE mode or interrupt request events
  - short reset sequence configuration
  - bidirectional reset behavior configuration
  - selection of alternate boot via the backup SRAM on STANDBY mode exit
  - boot mode capture on RESET deassertion

- ME
  - control of the available modes by the ME_ME register
  - definition of various device mode configurations by the ME_<mode>_MC registers
  - control of the actual device mode by the ME_MCTL register
  - capture of the current mode and various resource status within the contents of the ME_GS register
  - optional generation of various mode transition interrupts
  - status bits for each cause of invalid mode transitions
  - peripheral clock gating control based on the ME_RUN_PC0…7, ME_LP_PC0…7, and ME_PCTL0…143 registers
  - capture of current peripheral clock gated/enabled status
- PCU
  - support for 3 power domains
  - support for device modes RESET, DRUN, SAFE, TEST, RUN0…3, HALT, STOP, and STANDBY
  - power states updating on each mode change and on system wakeup
  - a handshake mechanism for power state changes thus guaranteeing operable voltage maps the VREG registers to the MC_PCU address space
- CAN Sampler
  - Store 384 samples, equivalent to 48 CAN bit @ 8 samples/bit
  - Sample frequency from 500 kHz up to 16 MHz, equivalent at 8 samples/bit to CAN baud rates of 62.5 Kbps to 2 Mbps
  - User selectable CAN Rx sample port [CAN0RX-CAN5RX]
  - 16 MHz fast internal RC oscillator clock
  - 5-bit clock prescaler
  - Configurable trigger mode (immediate, next frame)
  - Flexible samples processing by software
  - Very low power consumption
- CTU
  - Single cycle delayed trigger output. The trigger output is a combination of 64 (generic value) input flags/events connected to different timers in the system.
  - One event configuration register dedicated to each timer event allows to define the corresponding ADC channel.

  - Acknowledgment signal to eMIOS/PIT for clearing the flag
  - Synchronization with ADC to avoid collision
- RTC
  - 3 selectable counter clock sources
    - SIRC (128 kHz)
    - SXOSC (32 KHz)
    - FIRC (16 MHz)
  - Optional 512 prescaler and optional 32 prescaler
  - 32-bit counter
    - Supports times up to 1.5 months with 1 ms resolution
    - Runs in all modes of operation
    - Reset when disabled by software and by POR
  - 12-bit compare value to support interrupt intervals of 1 s up to greater than 1 hr with 1 s resolution
  - RTC compare value changeable while counter is running
  - RTC status and control register are reset only by POR
  - Autonomous periodic interrupt (API)
    - 10-bit compare value to support wakeup intervals of 1.0 ms to 1 s
    - Compare value changeable while counter is running
  - Configurable interrupt for RTC match, API match, and RTC rollover
  - Configurable wakeup event for RTC match, API match, and RTC rollover
- PIT
  - Timers can generate interrupts
  - All interrupts are maskable
  - Independent timeout periods for each timer
- STM
  - One 32-bit up counter with 8-bit prescaler
  - Four 32-bit compare channels
  - Independent interrupt source for each channel
  - Counter can be stopped in debug mode
- SWT
  - 32-bit time-out register to set the time-out period

  - The unique SWT counter clock is the undivided slow internal RC oscillator 128 kHz (SIRC), no other clock source can be selected
  - Programmable selection of window mode or regular servicing
  - Programmable selection of reset or interrupt on an initial time-out
  - Master access protection
  - Hard and soft configuration lock bits
  - The SWT is started on exit of power-on phase (RGM phase 2) to monitor flash boot sequence phase. It is then reset during RGM phase3 and optionally enabled when platform reset is released depending on value of flash user option bit 31 (WATCHDOG_EN).
- ECSM
  - Program-visible information on the device configuration and revision
  - Registers for capturing information on memory errors due to error-correction codes
  - Registers to specify the generation of single- and double-bit memory data inversions for test purposes to check ECC protection
  - Configuration for additional SRAM WS for system frequency above 64 + 4% MHz
- SSCM
  - System Configuration and Status
    - Memory sizes/status
    - Microcontroller Mode and Security Status (including censorship and serial boot information)
    - Search Code Flash for bootable sector
    - Determine boot vector
  - Device identification information (MCU ID Registers)
  - Debug Status Port enable and selection
  - Bus and peripheral abort enable/disable
- WKUP
  - Non-maskable interrupt support with
    - 1 NMI source with bypassable glitch filter
    - Independent interrupt destination: non-maskable interrupt, critical interrupt, or machine check request
    - Edge detection
  - External wakeup/interrupt support with
    - 3 system interrupt vectors for up to 18 interrupt sources

    - Analog glitch filter per each wakeup line
    - Independent interrupt mask
    - Edge detection
    - Configurable system wakeup triggering from all interrupt sources
    - Configurable pullup
  - On-chip wakeup support
    - 2 wakeup sources
    - Wakeup status mapped to same register as external wakeup/interrupt status
- CMU
  - FIRC, SIRC, SXOSC oscillator frequency measurement using FXOSC as reference clock
  - External oscillator clock monitoring with respect to FIRC_clk/n clock
  - FMPLL clock frequency monitoring for a high and low frequency range with FIRC as reference clock
  - Event generation for various failures detected inside monitoring unit
- DMA
  - 32 channels support independent 8-bit, 16-bit, or 32-bit single value or block transfers
  - Supports variable sized queues and circular queues
  - Source and destination address registers are independently configured to post-increment or remain constant
  - Each transfer is initiated by a peripheral, CPU, or eDMA channel request
  - Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- EBI
  - Two asynchronous active-low chip selects can be independently programmed with various features.
  - Support 256Mbyte block sizes for per chip select.
  - Support for 8-bit, 16-bit, and 32-bit devices for per chip select.

1.3 Block Diagram

Figure 1-1 is a block diagram of the system view.

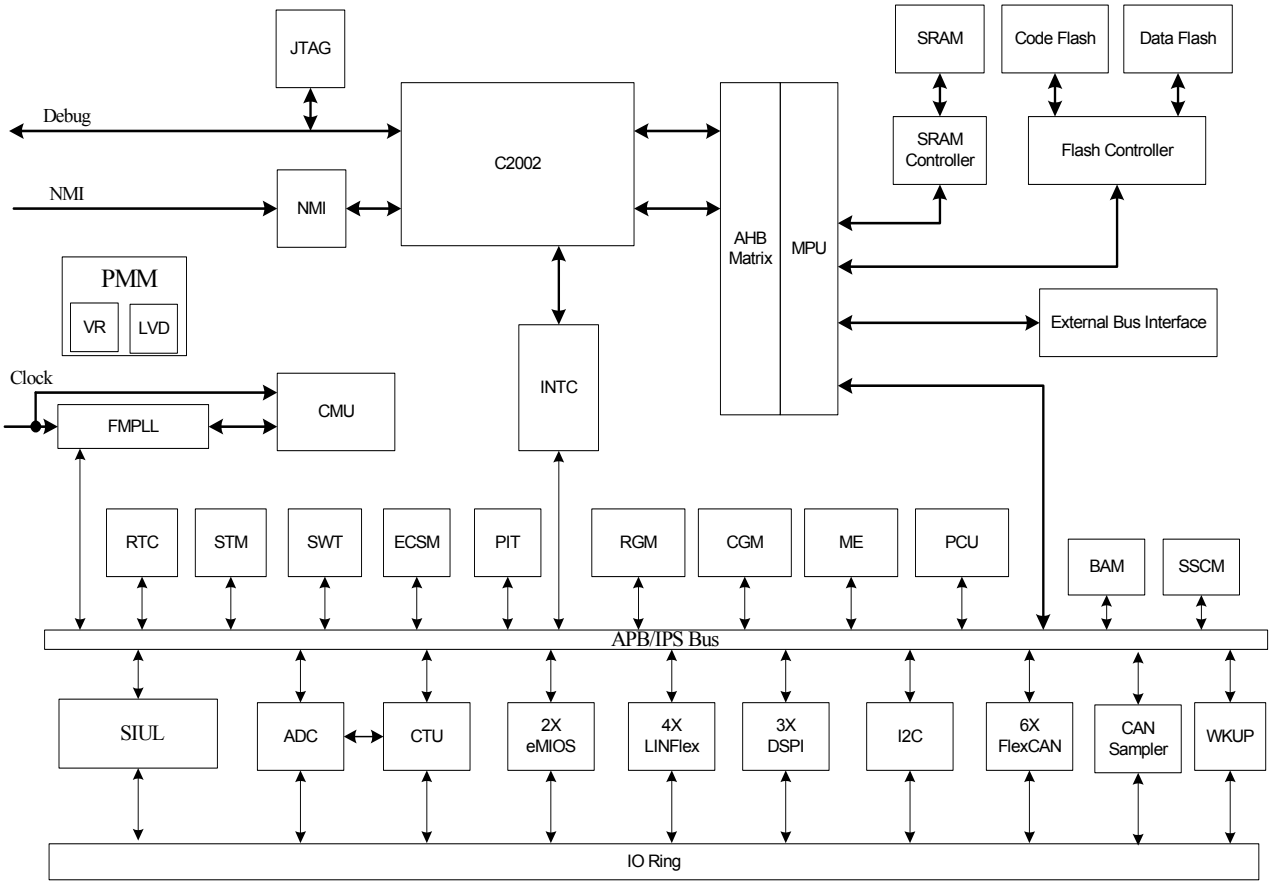

Figure 1-1 Block Diagram

Section 2 Package pinouts and signal descriptions

2.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions,please refer to the device reference manual.

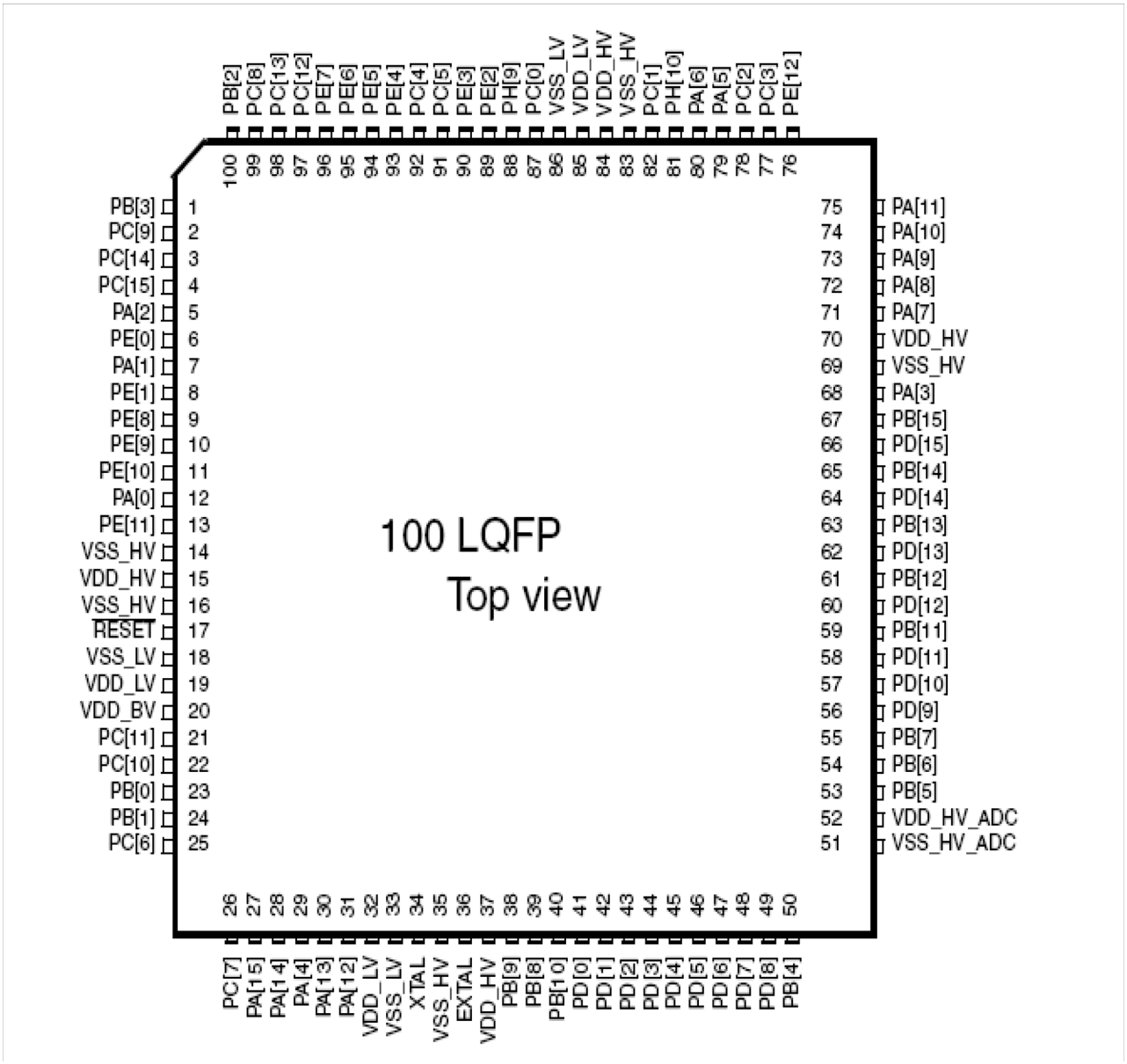

Figure 2-1 LQFP 100-pin configuration

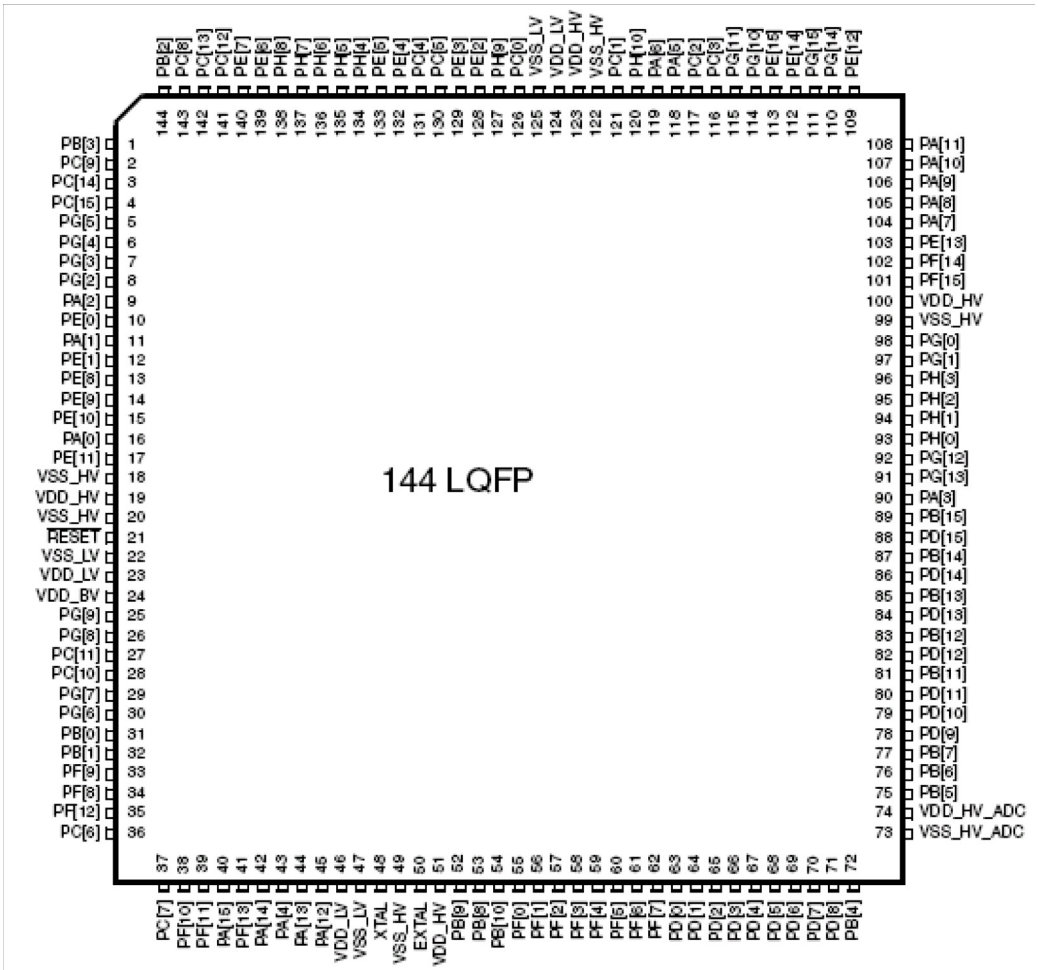

Figure 2-2 LQFP 144-pin configuration

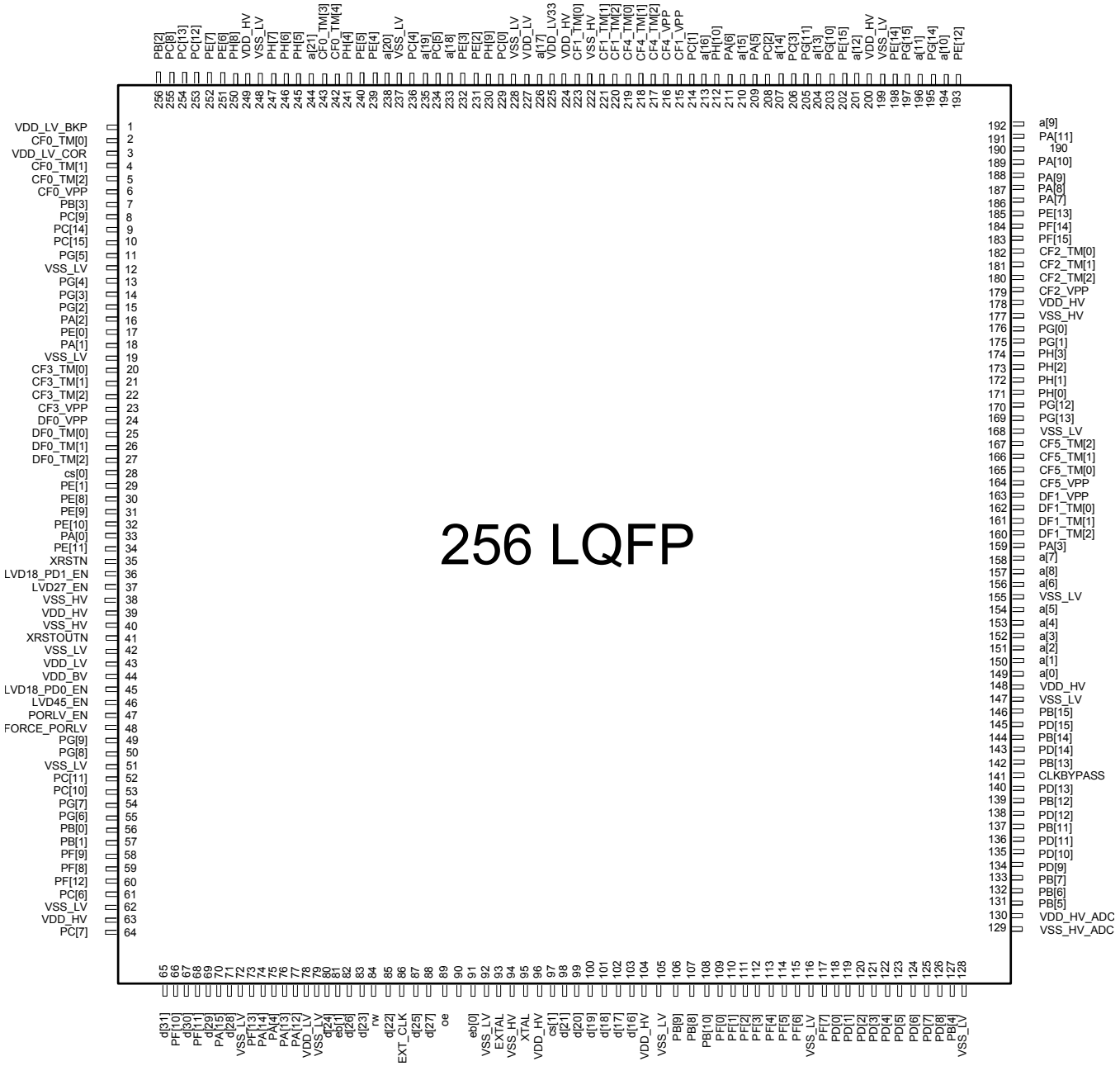

Figure 2-3 LQFP 256-pin configuration

Note:

Availability of port pin alternate functions depends on product selection.

2.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.

2.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Dedicated VDD_LV/VSS_LV supply pairs are used for 1.8 V regulator stabilization.

Table 2-1Voltage supply pin descriptions

Port pin	Function	Pin number		
		100 LQFP	144 LQFP	256 LQFP
VDD_HV	Digital supply voltage	15, 37, 70, 84	19, 51, 100, 123	39, 63, 96, 104,148,178,200,224, 249
VSS_HV	Digital ground	14, 16, 35, 69, 83	18, 20, 49, 99, 122	38, 40, 94, 177, 222
VDD_LV	1.8V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest VSS_LV pin.[1]	19, 32, 85	23, 46, 124	43, 78, 227

VSS_LV	1.8V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest VDD_LV pin.[1]	18, 33, 86	22, 47, 125	12, 19, 42,51,62,72,79,92,105,116,128,147,155,168,199,228,237,248
VDD_BV	Internal regulator supply voltage	20	24	44
VSS_HV_ADC	Reference ground and analog ground for the ADC	51	73	129
VDD_HV_ADC	Reference voltage and analog supply for the ADC	52	74	130

[1]A decoupling capacitor must be placed between each of the VDD_LV/VSS_LV supply pairs to ensure stable voltage.

2.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow

M = Medium

I = Input only with analog feature

J = Input/Output (‘S’ pad) with analog feature

X = Oscillator

2.5 System pins

The system pins are listed in **Table 2-2**.

Table 2-2 System pin descriptions

System pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					100 LQFP	144 LQFP	256 LQFP
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE	17	21	35

EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	X	Tristate	36	50	95
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	I	X	Tristate	34	48	93

2.6 Functional ports

The functional port pins are listed in **Table 2-2**.

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKUP[19][3]	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	M	Tristate	12	16	33[4]
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI[5] WKUP[2][3]	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	7	11	18
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKUP[3][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	5	9	16
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	68	90	159

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKUP[9][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	29	43	75
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	79	118	209
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	80	119	211
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	71	104	186
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	72	105	187
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	73	106	188
PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	74	107	189

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	75	108	191
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	S	Tristate	31	45	77
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	30	44	76
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 — EIRQ[4]	SIUL DSPI_0 DSPI_0 — SIUL	I/O I/O I/O — I	M	Tristate	28	42	74
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 — WKUP[10][3]	SIUL DSPI_0 DSPI_0 — WKPU	I/O I/O I/O — I	M	Tristate	27	40	70
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	M	Tristate	23	31	56
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKUP[4][3] CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	S	Tristate	24	32	57

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA —	SIUL LINFlex_0 I2C_0 —	I/O O I/O —	M	Tristate	100	144	256
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — — —	GPIO[19] — SCL — WKUP[11][3] LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	S	Tristate	1	1	7
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — GPI[0]	SIUL — — — ADC	I — — — I	I	Tristate	50	72	127
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — GPI[1]	SIUL — — — ADC	I — — — I	I	Tristate	53	75	131
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — GPI[2]	SIUL — — — ADC	I — — — I	I	Tristate	54	76	132
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — GPI[3]	SIUL — — — ADC	I — — — I	I	Tristate	55	77	133
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ANS[0] OSC32K_XTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	39	53	107

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ANS[1] OSC32K_EXTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	38	52	106
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKUP[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	40	54	108
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	59	81	137
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	61	83	139
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	63	85	142
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	65	87	144
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	67	89	146

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PC[0][8]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	87	126	229
PC[1][8]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO[9] —	SIUL — JTAGC —	I/O — O —	M	Tristate	82	121	214
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M	Tristate	78	117	208
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	77	116	206
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 CAN3RX	SIUL — — — DSPI_1 FlexCAN_3	I/O — — — I I	M	Tristate	92	131	236
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX — EIRQ[7]	SIUL DSPI1 FlexCAN_3 — SIUL	I/O O O — I	M	Tristate	91	130	234
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	25	36	61

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKUP[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	26	37	64
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	99	143	255
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKUP[13][3]	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	8
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	22	28	53
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX WKUP[5][3]	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	21	27	52
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	97	141	253

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	254
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	3	9
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	4	4	10
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	41	63	118
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — GPI[5]	SIUL — — — ADC	I — — — I	I	Tristate	42	64	119
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — GPI[6]	SIUL — — — ADC	I — — — I	I	Tristate	43	65	120
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — GPI[7]	SIUL — — — ADC	I — — — I	I	Tristate	44	66	121

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — GPI[8]	SIUL — — — ADC	I — — — I	I	Tristate	45	67	122
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — GPI[9]	SIUL — — — ADC	I — — — I	I	Tristate	46	68	123
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — GPI[10]	SIUL — — — ADC	I — — — I	I	Tristate	47	69	124
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — GPI[11]	SIUL — — — ADC	I — — — I	I	Tristate	48	70	125
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — GPI[12]	SIUL — — — ADC	I — — — I	I	Tristate	49	71	126
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — GPI[13]	SIUL — — — ADC	I — — — I	I	Tristate	56	78	134
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — GPI[14]	SIUL — — — ADC	I — — — I	I	Tristate	57	79	135

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — GPI[15]	SIUL — — — ADC	I — — — I	I	Tristate	58	80	136
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ANS[4]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	60	82	138
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ANS[5]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	62	84	140
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ANS[6]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	64	86	143
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ANS[7]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	66	88	145
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX WKUP[6][3]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	6	10	17
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	8	12	29

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS_0 — — DSPI_1	I/O I/O — — I	M	Tristate	89	128	231
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	90	129	232
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	93	132	239
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	94	133	240
PE[6]	PCR[70]	AF0 AF1 AF2 AF3	GPIO[70] E0UC[22] CS3_0 MA[1]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	95	139	251
PE[7]	PCR[71]	AF0 AF1 AF2 AF3	GPIO[71] E0UC[23] CS2_0 MA[0]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	96	140	252
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	13	30

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKUP[7][3] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	10	14	31
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 — EIRQ[10]	SIUL LINFlex_3 DSPI_1 — SIUL	I/O O O — I	S	Tristate	11	15	32
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] — CS4_1 — LIN3RX WKUP[14][3]	SIUL — DSPI_1 — LINFlex_3 WKPU	I/O — O — I I	S	Tristate	13	17	34
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — E1UC[19] — SIN_2 EIRQ[11]	SIUL — eMIOS_1 — DSPI_2 SIUL	I/O — I/O — I I	S	Tristate	76	109	193
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	103	185
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	S	Tristate	—	112	198

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	113	202
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ANS[8]	SIUL eMIOS_0 DSPI_1 — ADC	I/O I/O O — I	J	Tristate	—	55	109
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ANS[9]	SIUL eMIOS_0 DSPI_1 — I	I/O I/O O — I	J	Tristate	—	56	110
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ANS[10]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O I/O — I	J	Tristate	—	57	111
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ANS[11]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	58	112
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ANS[12]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	59	113
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ANS[13]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	60	114

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] — — ANS[14]	SIUL eMIOS_0 — — ADC	I/O I/O — — I	J	Tristate	—	61	115
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — — — ANS[15]	SIUL — — — ADC	I/O — — — I	J	Tristate	—	62	117
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	34	59
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — —	GPIO[89] — CS5_0 — CAN2RX CAN3RX	SIUL — DSPI_0 — FlexCAN_2 FlexCAN_3	I/O — O — I I	S	Tristate	—	33	58
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] — — —	SIUL — — —	I/O — — —	M	Tristate	—	38	66
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 —	GPIO[91] — — — WKUP[15][3]	SIUL — — — WKPU	I/O — — — I	S	Tristate	—	39	68
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	35	60

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 —	GPIO[93] E1UC[26] — — WKUP[16][3]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	41	73
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_4	I/O O I/O O	M	Tristate	—	102	184
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] — — — CAN1R CAN4RX EIRQ[13]	SIUL — — — FlexCAN_1 FlexCAN_4 SIUL	I/O — — — I I I	S	Tristate	—	101	183
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	98	176
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — CAN5RX EIRQ[14]	SIUL — eMIOS_1 — FlexCAN_5 SIUL	I/O — I/O — I I	S	Tristate	—	97	175
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	8	15
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] — — WKUP[17][3]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	7	14

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	6	13
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 —	GPIO[101] E1UC[14] — — WKUP[18][3]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	5	11
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	30	55
PG[7]	PCR[103]	AF0 AF1 AF2 AF3	GPIO[103] E1UC[16] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	29	54
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] — CS0_2 EIRQ[15]	SIUL eMIOS_1 — DSPI_2 SIUL	I/O I/O — I/O I	S	Tristate	—	26	50
PG[9]	PCR[105]	AF0 AF1 AF2 AF3	GPIO[105] E1UC[18] — SCK_2	SIUL eMIOS_1 — DSPI_2	I/O I/O — I/O	S	Tristate	—	25	49
PG[10]	PCR[106]	AF0 AF1 AF2 AF3	GPIO[106] E0UC[24] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	114	203

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	115	205
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	92	170
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	91	169
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	110	195
PG[15]	PCR[111]	AF0 AF1 AF2 AF3	GPIO[111] E1UC[1] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	111	197
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	93	171
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	M	Tristate	—	94	172

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	95	173
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	96	174
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	134	241
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	135	245
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC	I/O I/O — O	M	Tristate	—	136	246
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	137	247
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	138	250

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
PH[9][8]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	88	127	230
PH[10][8]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	81	120	212
A[0]	—	—	—	CEBI	O	S	Output	—	—	149
A[1]	—	—	—	CEBI	O	S	Output	—	—	150
A[2]	—	—	—	CEBI	O	S	Output	—	—	151
A[3]	—	—	—	CEBI	O	S	Output	—	—	151
A[4]	—	—	—	CEBI	O	S	Output	—	—	153

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
A[5]	—	—	—	CEBI	O	S	Output	—	—	154
A[6]	—	—	—	CEBI	O	S	Output	—	—	156
A[7]	—	—	—	CEBI	O	S	OutputOutput	—	—	157
A[8]	—	—	—	CEBI	O	S	Output	—	—	158
A[9]	—	—	—	CEBI	O	S	Output	—	—	192
A[10]	—	—	—	CEBI	O	S	Output	—	—	194
A[11]	—	—	—	CEBI	O	S	Output	—	—	196

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
A[12]	—	—	—	CEBI	O	S	Output	—	—	201
A[13]	—	—	—	CEBI	O	S	Output	—	—	204
A[14]	—	—	—	CEBI	O	S	Output	—	—	207
A[15]	—	—	—	CEBI	O	S	Output	—	—	210
A[16]	—	—	—	CEBI	O	S	Output	—	—	213
A[17]	—	—	—	CEBI	O	S	Output	—	—	226
A[18]	—	—	—	CEBI	O	S	Output	—	—	233

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
A[19]	—	—	—	CEBI	O	S	Output	—	—	235
A[20]	—	—	—	CEBI	O	S	Output	—	—	238
A[21]	—	—	—	CEBI	O	S	Output	—	—	244
CS[0]	—	—	—	CEBI	O	S	Output	—	—	28
CS[1]	—	—	—	CEBI	O	S	Output	—	—	97
D[16]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	103
D[17]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	102

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
D[18]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	101
D[19]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	100
D[20]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	99
D[21]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	98
D[22]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	85
D[23]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	83
D[24]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	80

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
D[25]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	87
D[26]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	82
D[27]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	88
D[28]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	71
D[29]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	69
D[30]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	67
D[31]	—	—	—	CEBI	I/O	S	Input, weak pull-up	—	—	65

Table 2-3Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number		
								100 LQFP	144 LQFP	256 LQFP
EB[0]	—	—	—	CEBI	O	S	Output	—	—	91
EB[1]	—	—	—	CEBI	O	S	Output	—	—	81
OE	—	—	—	CEBI	O	S	Output	—	—	89
RW	—	—	—	CEBI	O	S	Output	—	—	84

NOTES:

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 -> AF0; PCR.PA = 01 -> AF1; PCR.PA = 10 -> AF2; PCR.PA = 11 -> AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to ‘1’, regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as “—”.
2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI.PADSELx bitfields inside the SIUL module.
3. All WKUP pins also support external interrupt capability. See wakeup unit chapter for further details.
4. 256 LQFP contains pads which may not be available in other packages.
5. NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.
6. “Not applicable” because these functions are available only while the device is booting. Refer to BAM chapter of the reference manual for details.
7. Value of PCR.IBE bit must be 0
8. Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO. PC[0:1] are available as JTAG pins (TDI and TDO respectively). PH[9:10] are available as JTAG pins (TCK and TMS respectively). If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.

Package pinouts and signal descriptions

Section 3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins. The parameters listed in the following tables represent the characteristics of the device and its demands on the system. In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in **Table 3-1** are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3-1 Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE:The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.3.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. **Table 3-2** shows how NVUSRO[PAD3V5V] controls.the device configuration. Not support in current design.

Table 3-2 PAD3V5V field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

NOTE:3.3V power supply is not support in current version, all the electrical characteristics based on 3.3V supply mentioned below are not guaranteed.

3.3.2 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. **Table 3-3** shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 3-3 WATCHDOG_EN field description

Value[1]	Description
0	Disable after reset
1	Enable after reset

1 Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.4 Absolute maximum ratings

Table 3-4Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	-0.3	6.0	V
V_{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—		6.0	V
			Relative to V_{DD}	-0.3	V_{DD}+0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}-0.1	V_{SS}+0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	V_{DD} -0.3	V_{DD}+0.3	
$T_{STORAGE}$	SR	Storage temperature	—	-55	150	°C

NOTE: ***Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN} > V_{DD} or V_{IN} < V_{SS}), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.***

3.5 Recommended operating conditions

Table 3-5Recommended operating conditions (5.0 V)

Symbol		Parameter Conditions		Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD}-0.1	V_{DD}+0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}-0.1	V_{SS}+0.1	V
V_{DD_ADC}[4]	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop2	3.0	5.5	
			Relative to V_{DD}	V_{DD}-0.1	V_{DD}+0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}-0.1	—	V
			Relative to V_{DD}	—	V_{DD}+0.1	

NOTES:

1. 1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.
3. 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

NOTE:RAM data retention is guaranteed with V_{DD_LV} not below 1.62 V.

3.6 Electrical Characteristics

特性	符号	条件除另有规定外， V_{DD_HV}=5.0V； V_{DD_HV}=5.5V； V_{DD_HV}=4.5V -40℃ ≤ T_A ≤ 125℃	条件	极限值		单位
				最小	最大	
工作电流 [a]	I_{DDRUN}[1]	f_{CPU}= 48 MHz	T4 T5 T6[b]	0	100	mA
工作电流 [a]	I_{DDRUN}[1]	f_{CPU}= 64 MHz	T4 T5 T6[b]	0	125	mA
工作电流 [a]	I_{DDHALT}[2]	Slow internalRC oscillator(128 kHz) Running, TA = 125° C	T4 T5 T6[b]	0	25	mA
工作电流 [a]	I_{DDSTOP}[3]	Slow internalRC oscillator(128 kHz) running, TA = 25° C	T4 T5 T6[b]	0	1.2	mA
工作电流 [a]	I_{DDSTOP}[3]	Slow internalRC oscillator(128 kHz) running, TA = 125° C	T4 T5 T6[b]	0	1.2	mA
静态电流 [a]	$I_{DDSTDBY1}$[4]	Slow internalRC oscillator(128 kHz) runnin, TA = 25° C	T1 T2 T3[b]	0	60	uA
静态电流 [a]	$I_{DDSTDBY1}$[4]	Slow internalRC oscillator(128 kHz) runnin, TA = 125° C	T1 T2 T3[b]	0	1000	uA
静态电流 [a]	$I_{DDSTDBY2}$[5]	Slow internalRC oscillator(128 kHz) Runnin, TA = 25° C	T1 T2 T3[b]	0	100	uA
静态电流 [a]	$I_{DDSTDBY2}$[5]	Slow internalRC oscillator(128 kHz) runnin, TA = 125° C	T1 T2 T3[b]	0	1000	uA
输出高电平 (LOW)	V_{OH}	IOH = -2mA,VDD_HV =4.5V,PAD3V5V = 0	T1 T2 T3[b]	0.8* V_{DD-HV}	V_{DD-HV}	V
		IOH = -2 mA, VDD_HV =4.5V, PAD3V5V=1		0.8* V_{DD-HV}	V_{DD-HV}	V
		IOH = -1 mA, VDD_HV= 3.3 V,PAD3V5V=1		V_{DD-HV}-0.8	V_{DD-HV}	V
输出低电平 (LOW)	V_{OL}	IOL = 1 mA, VDD_HV= 3.3 V,PAD3V5V = 1	T1 T2 T3[b]	0	0.5	V
输出高电平 (MEDIUM)	V_{OH}	IOH = −2mA,VDD_HV=4.5V,PAD3V5V = 0	T1 T2 T3[b]	0.8* V_{DD-HV}	V_{DD-HV}	V
输出低电平 (MEDIUM)	V_{OL}	IOL = 2 mA, VDD_HV=4.5V,PAD3V5V = 0		0	0.5	V
上拉电流	I_{wpu}	VIN = VIL, VDD_HV= 5.0 V,PAD3V5V = 0	T1 T2 T3[b]	-200	-80	μA
		VIN = VIL, VDD_HV= 3.3 V,PAD3V5V = 1		-200	-80	μA
下拉电流	I_{WPD}	VIN = VIH, VDD_HV= 5.0 V,PAD3V5V = 0		80	200	μA
		VIN = VIH, VDD_HV= 3.3 V,PAD3V5V = 1		80	200	μA

电压校准器输出电压	VLDO_CORE	Main regulator outputvoltage	T1 T2 T3[b]	1.782	1.818	V
低电压侦测	VLVDHV3L		T1 T2 T3[b]	2.6	3.1	V
	VLVDHV5L		T1 T2 T3[b]	3.7	4.4	V
高电平输入漏电流	I_{IH}		T1 T2 T3[b]	-1000	1000	nA
低电平输入漏电流	I_{IL}			-1000	1000	nA
输入高电平电压	V_{IH}		T1 T2 T3[b]	0.65*V_{DD-HV}	V_{DD-HV}	V
输入低电平电压	V_{IL}			0	0.35*V_{DD5V}	V
输入高电平电压(EXTAL)	V_{IH}	Oscillator bypassmode	T1 T2 T3[b]	0.65*V_{DD-HV}	V_{DD-HV}	V
输入低电平电压(EXTAL)	V_{IL}			0	0.35*V_{DD5V}	V

差分非线性 [c]	*DNL*	ADC 转换速率为 1MS/s，ADC 时钟频率=16MHz，ADC 转换周期=16*时钟周期	T1 T2 T3[b]	-3	3	LSB
积分非线性 [c]	*INL*			-3	3	LSB
ADC 动作电流	AI_{CC}	器件处于 ADC 动作状态	T4 T5 T6[b]	0	10	mA
ADC 静态电流	AI_{CC}	器件处于 ADC 静止状态	T1 T2 T3[b]	0	20	uA
内建自测试	*DFT*	具体测试项详见附录表 A.1。	T7 T8A T8B[b]			
扫描链测试	*DFT*	具体测试项详见附录表 A.1。				
功能测试	*FUNC*	具体测试项详见附录表 C.1。				
闪存测试	*FLASH*	测具体测试项详见附录表 B.1。				
PLL 频率	*FREQ*	外部晶振=4MHz，经过 PLL 倍频至 64MHz，8 分频后从 IO 输出 8MHz	T4 T5 T6[b]	7.96	8.04	MHz
		外部晶振=4MHz，经过 PLL 倍频至 80MHz，8 分频后从 IO 输出 10 MHz		9.95	10.05	MHz
		外部晶振=16MHz，经过 PLL 倍频至 64MHz，8 分频后从 IO 输出 8MHz		7.96	8.04	MHz
		外部晶振=16MHz，经过 PLL 倍频至 80MHz，8 分频后从 IO 输出 10 MHz		9.95	10.05	MHz
快速外部晶体振荡器	*FREQ*	快速外部晶体振荡器输出时钟频率 FXOSC	T4 T5 T6 [b]	15.9	16.1	MHz
快速内部 RC 振荡器	*FREQ*	快速内部 RC 振荡器输出时钟频率 FIRC	T4 T5 T6 [b]	15.84	16.25	MHz
低速内部 RC 振荡器	*FREQ*	低速内部 RC 振荡器输出时钟频率 SIRC	T4 T5 T6 [b]	122	134	KHz
RTC 频率	*FREQ*		T4 T5 T6 [b]	31	33	KHz

1. Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. SXOSC is on.

2. Data Flash Power Down. Code Flash in Low Power. SIRC (128 kHz) and FIRC (16 MHz) on. 16 MHz XTAL clock, SXOSC is off. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion.

3. Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, SXOSC/FXOSC is off. ULPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

4. ULPreg on, HPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

5. Only for the “P” classification: ULPreg on, HPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

[b] 电测试分组规则如下：

1) T1 分组：25℃下的静态试验
2) T2 分组：最高额定工作温度下的静态试验？
3) T3 分组：最低额定工作温度下的静态试验
4) T4 分组：25℃下的动态试验
5) T5 分组：最高额定工作温度下的动态试验
6) T6 分组：最低额定工作温度下的动态试验
7) T7 分组：25℃下的功能试验
8) T8A 分组：最高额定工作温度下的功能试验
9) T8B 分组：最低额定工作温度下的功能试验

[c] 模拟通道输入电压范围是-0.3V ~ 5.8V，ADC 参考电压高 4.5V~5.5V

Electrical characteristics

Section 4 Package characteristics

4.1 Package mechanical data

4.1.1 100 LQFP

4.1.2 144 LQFP

4.1.3 256 LQFP

Package characteristics

Section 5 Document revision history

Table 5-1 summarizes revisions to this document.

Table 5-1 Revision history

Revision	Date	Description of Changes
0.1	11-Nov-2014	Initial release.

Document revision history

Section 6 Abbreviations

Table 6-1 lists abbreviations used but not defined elsewhere in this document.

Table 6-1 Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Abbreviations