CCM3310S-T/TB
Advance Information
Rev 1.3

CMOS
Microcontroller Unit

C*Core R&D Center.

[redacted]

Release Number	Date	Author	Summary of Changes
1.0	2018/1/17	C*Core	1) New Created
1.1	2019/5/15	C*Core	1) modify operating temprature&intro for USB
1.2	2019/6/20	C*Core	1) adjusting the organization and format
1.3	2019/7/10	C*Core	1) add automotive application preliminary electircal characteristic description

Section 1 Introduction

Section 2 Signal Description

[redacted]

[redacted]

Section 1 Introduction

1.1 Introduction

The chip is a multi-purpose MCU based on the C*CORE C0 central processor unit (CPU). It is designed to act as a controller for information security application.

The operation frequency is 60MHZ.

1.2 Features

Features :

- C*CORE C0 processor :
  - 32-bit load/store reduced instruction set computer (RISC) architecture with fixed 16-bit instruction length
  - 16 entry 32-bit general-purpose register file
  - Efficient 3-stage execution pipeline, hidden from application software
  - Single-cycle instruction execution for many Instructions, three cycles for branches
  - Support for byte/halfword/word memory accesses
  - Embedded interrupt controller, support nested vector interrupts.
  - Single-cycle 32-bit x 32-bit hardware integer multiplier array

    3~13 cycles hardware integer divider array
  - The processor is implemented with several specific instructions to accelerate the fingerprint recognition programs. The instructions are grouped as:

    Multiply-accumulate in matrix of 8-bit numbers: umac8, smac8, dmac8

    Fix-point trigonometric functions: sincos, arctan

    2D vector rotation with saturation arithmetic: rotate, setsat, clrsat

    Tensor and complex number calculation: tensort, decompose, complexitp, tenmerge
- SWD debug support
- On-chip, 32K Bytes of static random-access memory (SRAM):

  - Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes
- On-chip, 16K Bytes of static read only memory (ROM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) read access.
- On-chip 256K Bytes embedded flash (EFLASH)
  - Memory Origanization: 64KX38+128X38
  - Reads of bytes, aligned halfwords (16 bits) and aligned words (32 bits)
  - Automated program and erase operation
  - Optional interrupt on command completion
  - Data Retention: 10 years under 85 degrees
  - Endurance: 100K cycles
- External interrupts supported(EPORT) :
  - Rising/falling edge select
  - Low-level sensitive
  - Ability for software generation of external interrupt event
  - Interrupt pins configurable as general-purpose I/O
- I2C Controller
  - Supports 10 bit addressing.
  - Supports Standard Mode, Fast Mode and High-Speed Mode
  - Software option to select between High-Speed mode and Standard/Fast mode
  - Compatibility with standard and fast-mode of I2C bus version 2.1 standard.
  - Multiple-master operation.
  - Software-programmable for one of 64 different serial clock frequencies.
  - Software-selectable acknowledge bit.
  - Interrupt-driven, byte-by-byte data transfer.
  - Arbitration-lost interrupt with automatic mode switching from master to slave.
  - Transfer completion and read configure interrupt.
  - Start and stop signal generation/detection.
  - Repeated START signal generation.

  - Acknowledge bit generation/detection.
  - Bus-busy detection.
  - Option slave address receiving enable when system clock stop mode
  - SCL or SDA line gpio function supported
- DMA Controller
  - Compliance to the AMBA Specification for easy integration into SoC implementation.
  - Four DMA channels. Each channel can support a unidirectional transfer. 16 DMA requests. The DMAC provides 6 peripheral DMA request lines.
  - Single DMA and burst DMA request signals. Each peripheral connected to the DMAC can assert either a burst DMA request or a single DMA request.
  - The DMA burst size is set by programming the DMAC.
  - Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
  - Scatter or gather DMA is supported through the use of linked lists.
  - Software programable DMA channel priority.
  - AHB slave DMA programming interface. The DMAC is programmed by writing to the DMA control registers over the AHB slave interface.
  - Two AHB bus masters for transferring data. These interfaces are used to transfer data when a DMA request goes active.
  - 32-bit AHB master bus width.
  - Incrementing or non-incrementing or decrease addressing for source and destination.
  - Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
  - Internal 16 word FIFO per channel.
  - Supports 8, 16, and 32-bit wide transactions.
  - Separate and combined DMA error and DMA count interrupt requests. An interrupt to the processor can be generated on a DMA error or when a DMA count has reached 0 (this is usually used to indicate that a transfer has finished). Three interrupt request signals are used to do this:
  - Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.

  - Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.
  - Test registers for use in block and integration system level testing.
  - Identification registers that uniquely identify the DMAC. These can be used by an operating system to automatically configure itself.
- Two Periodic interval timer :
  - 16-bit/32bit counter with modulus "initial count" register
  - Selectable as free running or count down
  - 16 selectable prescalers — 2^0 to 2^{15}
- Watchdog timer :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Time Counter :
  - Asynchronous 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Reset :
  - Separate reset in and reset out signals
  - Six sources of reset:

    Power-on reset

    Software reset

    Watchdog timer

    USI Reset

    Time Counter

    Power Attack Detect Reset
  - Status flag indicates source of last reset
- Serial communications interface (SCI):
  - Full-duplex operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver

  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- EDMAC
  - Support two channels
  - Programmable transfer total number
  - Programmable read buffer address and write buffer address
  - Multiple peripheral selectt
  - Support read, write and write then read transfer
- ISO7816 card interfaces (configuration to set Host or Device) :
  - Support of ISO7816-3
  - Support both card and card reader mode
  - Support T=0 and T=1 protocal
  - Half-duplex operation
  - 1 transmit buffer + 1 receive buffer
  - F/D selection(31,23.25, 46.5, 93, 186, 372,744,8,12,16,32,64,128,256,512)
  - 9-bit guard time counter (GTCNT)
  - 24 bits waiting time counter (WTCNT)
  - Programmable transmitter output polarity
  - Interrupt-driven operation with six flags:
    - Transmitter empty
    - Transmission complete
    - Receive full
    - ERROR
    - Start bit detected
    - Timeout on WT counter
    - Answer to Reset

  - Auto-character repetition on error signal detection in transmit mode
  - Auto-error signal generation on parity error detection in receive mode
  - Hardware parity checking
  - 1/16 bit-time noise detectio
  - General purpose, IO capability
- The LED Module:
  - To enable or disable the corresponding port, int[3], as an output port
  - To program the frequency of blink of the LED device
  - To program the dutycycle of blink of the LED device
  - A 20-bit prescaler reduces the 12 MHz clock to a 11.44 Hz pulse
  - A 4-bit counter determines the final frequency and dutycycle
- Serial peripheral interfaces (SPI) :
  - Master mode and slave mode configurable
  - Slave select output
  - Mode fault error flag with CPU interrupt capability
  - Control of SPI operation during doze mode
  - Reduced drive control for lower power consumption
  - Programmable interface operation for Freescale SPI or Texas Instruments synchronous serial interfaces
  - Separate transmit and receive FIFOs, each 8 bits wide and 8 locations deep
  - Programmable data frame size from 4 to 16 bits
  - Internal loopback test mode for diagnostic/debug testing
  - Standard FIFO-based interrupts and End-of-Transmission interrupt
  - Efficient transfers with DMA interface
  - Visibility into TX and RX FIFOs for ease of debugging
  - High Speed Mode for transfer timing adjustment
  - Serial clock with programmable polarity and phase
- Secure features
  - Internal power on reset
  - Voltage detector

  - Ligth detector
  - Power Glitch detector
  - Metal Shield protection
  - Temperature detector
  - Data encryption
  - Clock and reset pulse filtration
  - Safe optimized routing
- Crypto Accelerator module

  The CRYPTO Accelerator module supports popular public key cryptography algorithms (ECC/SM2/RSA) by implementing some large integer arithmetic operations in hardware.

  - Large operand size N integer arithmetic

    32 * R bits

    R is positive integer from 1 to 64
  - Programmable scalar or modulo operation

    Y = (A ^ E) mod N

    Y = (A + E) mod N

    Y = (A + A) mod N

    Y = (A - E) mod N

    Y = (A * R) mod N

    Y = (A * A * R) mod N

    Y = (A * E * R) mod N

    ECC2P

    ECCPQ
  - Discrete "sea-of-gates" implementation to protection against SPA/DPA and probing attacks
- AES module
  - Support AES encryption/decryption algorithm.
  - Support AES algorithm with 128/192/256 bits key
  - Support Electronic Code Book (ECB) mode operation ,CBC mode,OFB mode,CFB mode,and CTR(counter) mode operation
- SHA coprocessor

  - SM3(256)
  - SHA-0(160)
  - SHA-1(160)
  - SHA-224(224)
  - SHA-256(256)
  - Share hardware between different SHA processing
- SM4 module
  - Support SM4 algorithm with 128 bits key
  - Support ECB/CBC/CFB/OFB mode
- DES coprocessor
  - Support DES and Triple-DES encryption and decryption algorithm
  - Support DES algorithm with 64(56) bits key
  - Support Triple-DES algorithm with 128(112) bits or 192(168) bits key
  - Support ECB mode and CBC mode
  - Support several security countermeasures to prevent side channel attacks:

    Protection against SPA/DPA

    Protection against Hi_Order DPA

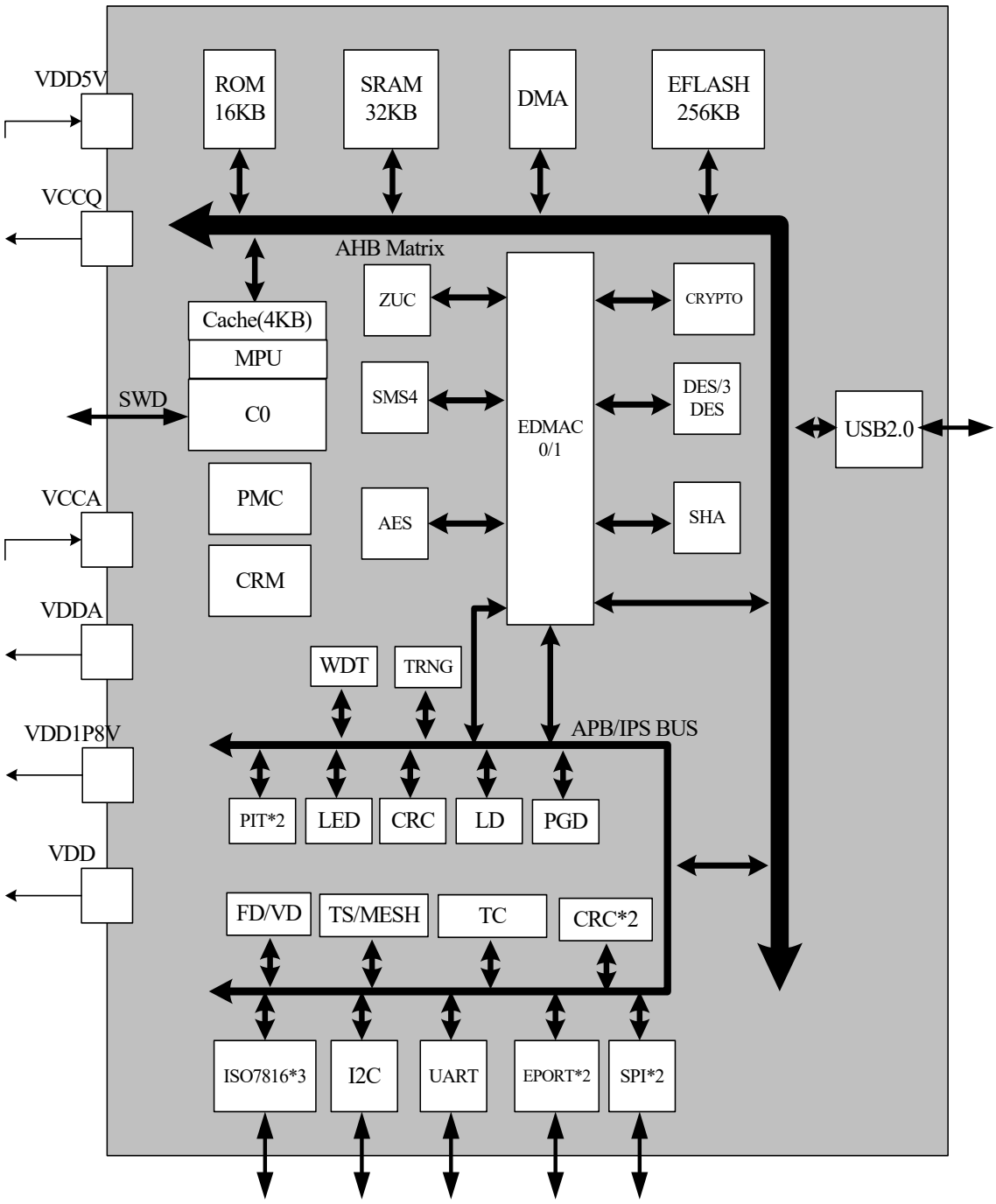
    Protection against DFA
- ZUC module
  - Support ZUC algorithm with 128 bits key
  - Support several security countermeasures to prevent side channel attacks:
  - Protection against SPA/DPA
  - Protection against Hi_Order DPA
  - Protection against DFA
- CRC coprocessor
  - Support CRC32 / CRC16 / CRC8
- TRNG(random number generator)
  - Rate: 4Mbps

- USB(high-speed function is supported only when external crystal 12MHz is used,if internal 12MHz osc is used,only support full-speed function)
  - Performs all transaction scheduling in hardware
  - Operates as a function controller for a USB peripheral in point-to-point communications with another USB function
  - Synchronous RAM interface for FIFOs
  - Certified compliant with the USB 2.0 standard for high-speed (480 Mbps) functions
  - Supports point-to-point communications with one high-, full- or low-speed device
  - Supports Suspend and Resume
  - Endpoint 0 supports control transfer and configurable for up to 7 additional Transmit endpoints and up to 7 additional Receive endpoints
  - Configurable FIFOs, including the option of dynamic FIFO sizing
  - Soft connect/disconnect option

1.3 Block Diagram

Figure 1-1 is a block diagram of the system.

Figure 1-1 Block Diagram



Section 2 Signal Description

2.1 Introduction

The chip is available in four types of package:

- SSOP28
- QFP48_R
- QFN48_N
- QFN32

2.2 Package Pinout Summary

Refer to:

- **Figure 2-1** for SSOP28 package
- **Figure 2-2** for QFP48_R package
- **Figure 2-3** for QFN48_N package
- **Figure 2-4** for QFN32 package
- **Table 2-1** for Signal Description for SSOP28.
- **Table 2-2** for Signal Description for QFP48_R.
- **Table 2-3** for Signal Description for QFN48_N.
- **Table 2-4** for Signal Description for QFN32.

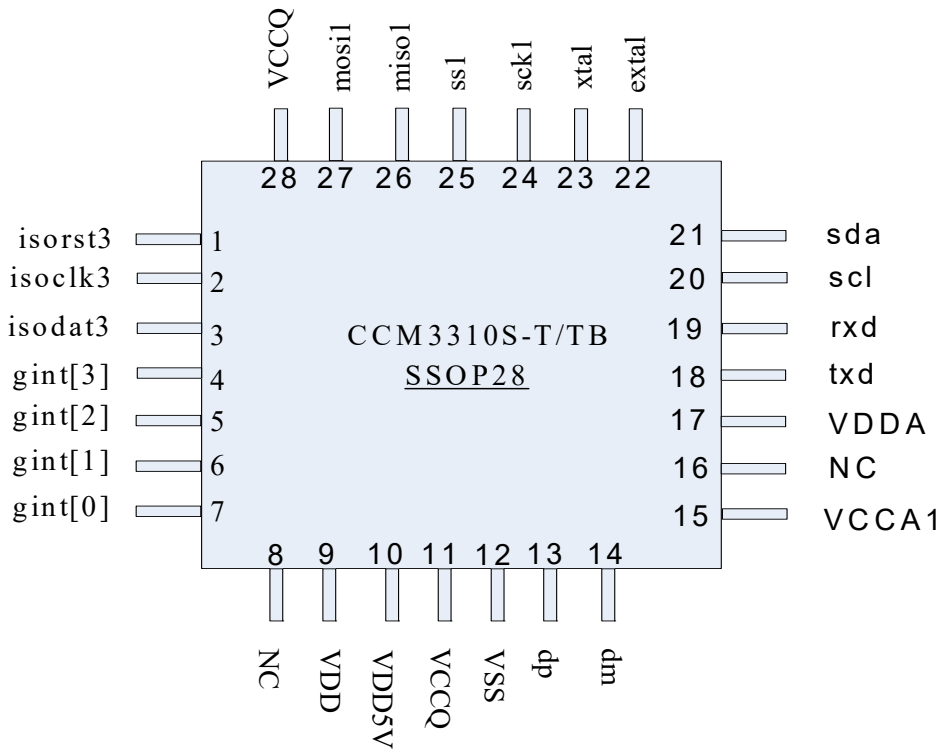


Figure 2-1 SSOP28 Package

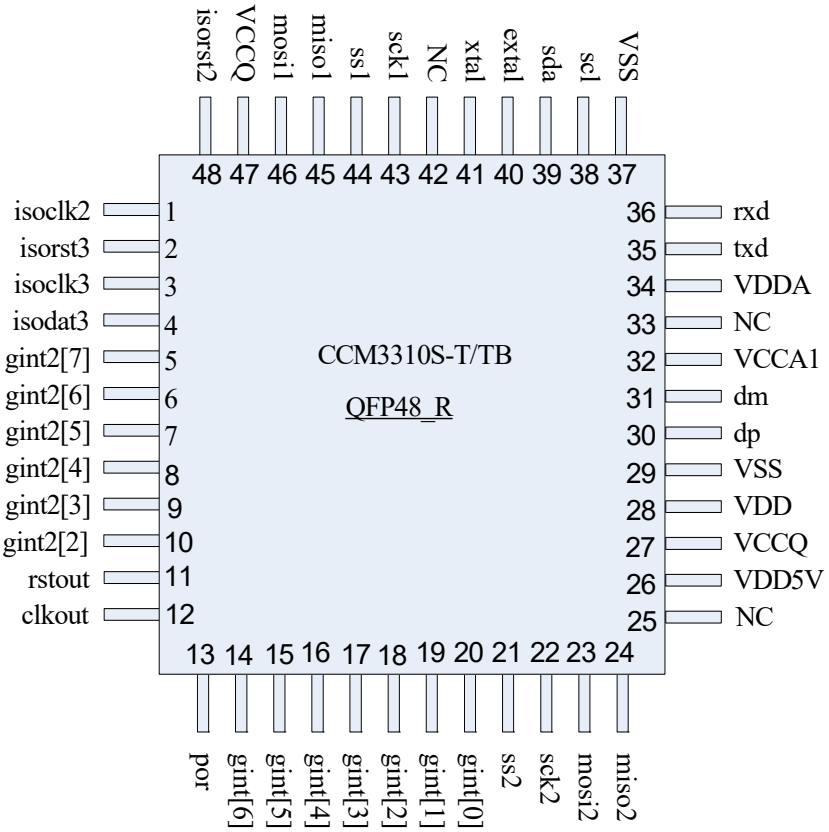


Figure 2-2 QFP48-R Package

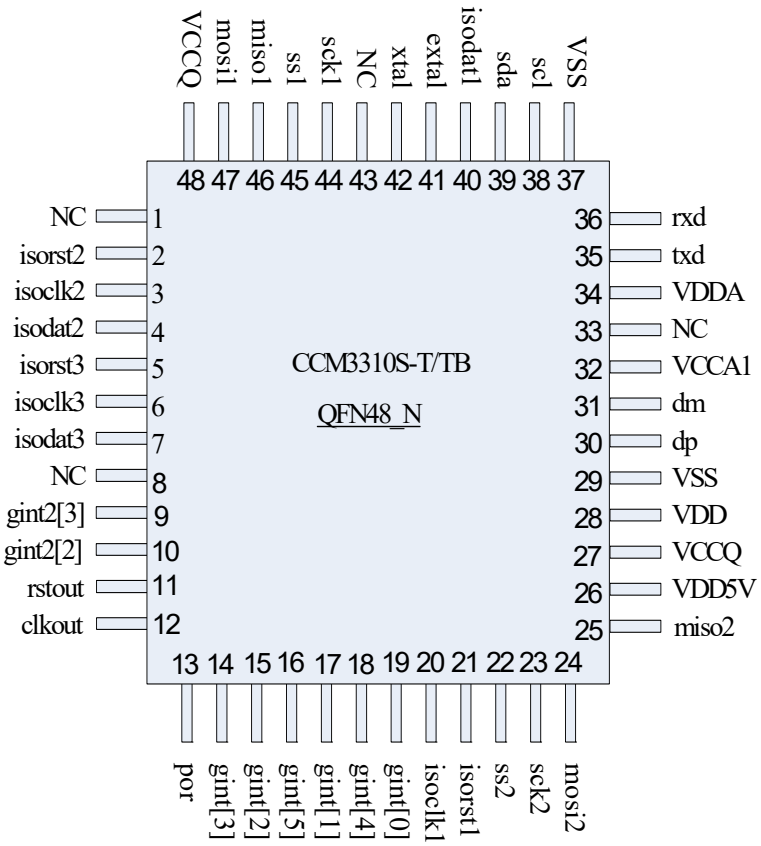


Figure 2-3 QFN48-N Package

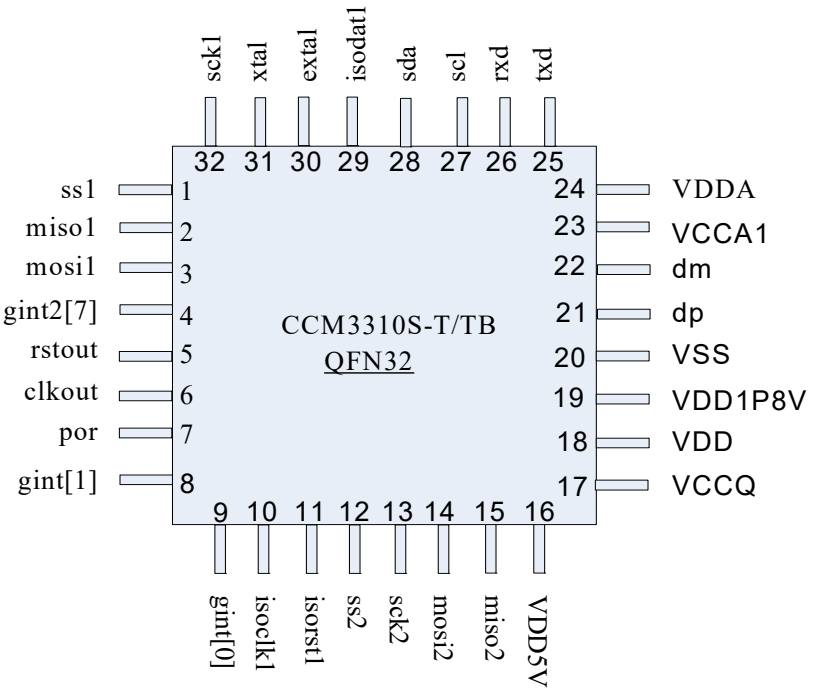


Figure 2-4 QFN32 Package

2.3 Signal Properties Summary

Table 2-1 Signal Description for SSOP28

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
Clock(2)						
extal	-	1	I	N	-	-
xtal	-	1	O	N	-	ST
Serial Periheral Interface(SPI1)(4)						
mosi1	-	1	I/O	Y	Pullup	ST/OD
miso1	-	1	I/O	Y	Pullup	ST/OD
sck1	-	1	I/O	Y	Pullup	ST/OD
$\overline{ss1}$	-	1	I/O	Y	Pullup	ST/OD
ISO-7816 Interface (USI1) (3)						
isoclk3	-	1	I/O	Y	Pullup	ST/OD
isodat3	-	1	I/O	Y	Pullup	ST/OD
isorst3	-	1	I/O	Y	Pullup	ST/OD
I2C Interface(2)						
scl	-	1	I/O	Y	Pullup	ST/OD
sda	-	1	I/O	Y	Pullup	ST/OD
SCI Interface(2)						
txd	-	1	I/O	Y	Pullup	ST/OD
rxd	-	1	I/O	Y	Pullup	ST/OD
Edge Port (EPORT) (4)						
gint[0]	-	1	I/O	Y	Pullup	ST/OD
gint[1]	-	1	I/O	Y	Pullup	ST/OD
gint[2]	-	1	I/O	Y	Pullup	ST/OD
gint[3]	-	1	I/O	Y	Pullup	ST/OD
USB(2)						
dp	-	1	I/O	N	-	-
dm	-	1	I/O	N	-	-
Power Supply(7)						
VCCQ	-	1	-	-	-	-
VDD	-	1	-	-	-	-

Table 2-1 Signal Description for SSOP28

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
VDD5V	-	1	-	-	-	-
VSS	-	1	-	-	-	-
VCCA1	-	1	-	-	-	-
VDDA	-	1	-	-	-	
AGND1	-	1	-	-	-	-

NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. Synchronized input used only if signal configured as a digital I/O.
3. All pullups are disconnected when the signal is programmed as an output.
4. All Not-Single-Chip I/O pins will be put into input mode and be connected to pullups.
5. Output driver type: ST = standard, SP = special, OD = standard driver with open-drain pulldown option selected.

Table 2-2 Signal Description for QFP48_R

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
Reset(2)						
por	-	1	O	N	Pullup	ST
rstout	-	1	O	N	Pullup	ST
Clock(3)						
extal	-	1	I	N	-	-
xtal	-	1	O	N	-	ST
clkout	-	1	O	N	-	-
Serial Periheral Interface(SPI1/2)(8)						
mosi1	-	1	I/O	Y	Pullup	ST/OD
miso1	-	1	I/O	Y	Pullup	ST/OD
sck1	-	1	I/O	Y	Pullup	ST/OD
$\overline{ss1}$	-	1	I/O	Y	Pullup	ST/OD
mosi2	-	1	I/O	Y	Pullup	ST/OD
miso2	-	1	I/O	Y	Pullup	ST/OD
sck2	-	1	I/O	Y	Pullup	ST/OD
$\overline{ss2}$	-	1	I/O	Y	Pullup	ST/OD
ISO-7816 Interface (USI/2/3) (5)						
isoclk2	-	1	I/O	Y	Pullup	ST/OD
isorst2	-	1	I/O	Y	Pullup	ST/OD
isoclk3	-	1	I/O	Y	Pullup	ST/OD
isodat3	-	1	I/O	Y	Pullup	ST/OD
isorst3	-	1	I/O	Y	Pullup	ST/OD
I2C Interface(2)						
scl	-	1	I/O	Y	Pullup	ST/OD
sda	-	1	I/O	Y	Pullup	ST/OD
SCI Interface(2)						
txd	-	1	I/O	Y	Pullup	ST/OD
rxd	-	1	I/O	Y	Pullup	ST/OD
Edge Port (EPORT) (13)						
gint[0]	-	1	I/O	Y	Pullup	ST/OD
gint[1]	-	1	I/O	Y	Pullup	ST/OD
gint[2]	-	1	I/O	Y	Pullup	ST/OD

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
gint[3]	-	1	I/O	Y	Pullup	ST/OD
gint[4]	-	1	I/O	Y	Pullup	ST/OD
gint[5]	-	1	I/O	Y	Pullup	ST/OD
gint[6]	-	1	I/O	Y	Pullup	ST/OD
gint2[2]	-	1	I/O	Y	Pullup	ST/OD
gint2[3]	-	1	I/O	Y	Pullup	ST/OD
gint2[4]	-	1	I/O	Y	Pullup	ST/OD
gint2[5]	-	1	I/O	Y	Pullup	ST/OD
gint2[6]	-	1	I/O	Y	Pullup	ST/OD
gint2[7]	-	1	I/O	Y	Pullup	ST/OD
USB2.0(2)						
dp	-	1	I/O	N	-	-
dm	-	1	I/O	N	-	-
Power Supply(7)						
VCCQ	-	1	-	-	-	-
VDD	-	1	-	-	-	-
VDD5V	-	1	-	-	-	-
VSS	-	1	-	-	-	-
VCCA1	-	1	-	-	-	-
VDDA	-	1	-	-	-	
AGND1	-	1	-	-	-	-

NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. Synchronized input used only if signal configured as a digital I/O.
3. All pullups are disconnected when the signal is programmed as an output.
4. All Not-Single-Chip I/O pins will be put into input mode and be connected to pullups.

5. Output driver type: ST = standard, SP = special, OD = standard driver with open-drain pulldown option selected.

Table 2-3 Signal Description for QFN48_N

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
Reset(2)						
por	-	1	O	N	Pullup	ST
rstout	-	1	O	N	Pullup	ST
Clock(3)						
extal	-	1	I	N	-	-
xtal	-	1	O	N	-	ST
clkout	-	1	O	N	-	-
Serial Periheral Interface(SPI1/2)(8)						
mosi1	-	1	I/O	Y	Pullup	ST/OD
miso1	-	1	I/O	Y	Pullup	ST/OD
sck1	-	1	I/O	Y	Pullup	ST/OD
$\overline{ss1}$	-	1	I/O	Y	Pullup	ST/OD
mosi2	-	1	I/O	Y	Pullup	ST/OD
miso2	-	1	I/O	Y	Pullup	ST/OD
sck2	-	1	I/O	Y	Pullup	ST/OD
$\overline{ss2}$	-	1	I/O	Y	Pullup	ST/OD
ISO-7816 Interface (USI/2/3) (9)						
isoclk1	-	1	I/O	Y	Pullup	ST/OD
isorst1	-	1	I/O	Y	Pullup	ST/OD
isodat1	-	1	I/O	Y	Pullup	ST/OD
isoclk2	-	1	I/O	Y	Pullup	ST/OD
isodat2	-	1	I/O	Y	Pullup	ST/OD
isorst2	-	1	I/O	Y	Pullup	ST/OD
isoclk3	-	1	I/O	Y	Pullup	ST/OD
isodat3	-	1	I/O	Y	Pullup	ST/OD
isorst3	-	1	I/O	Y	Pullup	ST/OD
I2C Interface(2)						
scl	-	1	I/O	Y	Pullup	ST/OD
sda	-	1	I/O	Y	Pullup	ST/OD
SCI Interface(2)						
txd	-	1	I/O	Y	Pullup	ST/OD
rxd	-	1	I/O	Y	Pullup	ST/OD

Signal Description

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
Edge Port (EPORT) (8)						
gint[0]	-	1	I/O	Y	Pullup	ST/OD
gint[1]	-	1	I/O	Y	Pullup	ST/OD
gint[2]	-	1	I/O	Y	Pullup	ST/OD
gint[3]	-	1	I/O	Y	Pullup	ST/OD
gint[4]	-	1	I/O	Y	Pullup	ST/OD
gint[5]	-	1	I/O	Y	Pullup	ST/OD
gint2[2]	-	1	I/O	Y	Pullup	ST/OD
gint2[3]	-	1	I/O	Y	Pullup	ST/OD
USB2.0(2)						
dp	-	1	I/O	N	-	-
dm	-	1	I/O	N	-	-
Power Supply(7)						
VCCQ	-	1	-	-	-	-
VDD	-	1	-	-	-	-
VDD5V	-	1	-	-	-	-
VSS	-	1	-	-	-	-
VCCA1	-	1	-	-	-	-
VDDA	-	1	-	-	-	
AGND1	-	1	-	-	-	-

NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. Synchronized input used only if signal configured as a digital I/O.
3. All pullups are disconnected when the signal is programmed as an output.
4. All Not-Single-Chip I/O pins will be put into input mode and be connected to pullups.

5. Output driver type: ST = standard, SP = special, OD = standard driver with open-drain pulldown option selected.

Table 2-4 Signal Description for QFN32

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
Reset(2)						
por	-	1	O	N	Pullup	ST
rstout	-	1	O	N	Pullup	ST
Clock(3)						
extal	-	1	I	N	-	-
xtal	-	1	O	N	-	ST
clkout	-	1	O	N	-	-
Serial Periheral Interface(SPI1/2)(8)						
mosi1	-	1	I/O	Y	Pullup	ST/OD
miso1	-	1	I/O	Y	Pullup	ST/OD
sck1	-	1	I/O	Y	Pullup	ST/OD
ss1	-	1	I/O	Y	Pullup	ST/OD
mosi2	-	1	I/O	Y	Pullup	ST/OD
miso2	-	1	I/O	Y	Pullup	ST/OD
sck2	-	1	I/O	Y	Pullup	ST/OD
ss2	-	1	I/O	Y	Pullup	ST/OD
ISO-7816 Interface (USI/2/3) (3)						
isoclk1	-	1	I/O	Y	Pullup	ST/OD
isorst1	-	1	I/O	Y	Pullup	ST/OD
isodat1	-	1	I/O	Y	Pullup	ST/OD
I2C Interface(2)						
scl	-	1	I/O	Y	Pullup	ST/OD
sda	-	1	I/O	Y	Pullup	ST/OD
SCI Interface(2)						
txd	-	1	I/O	Y	Pullup	ST/OD
rxd	-	1	I/O	Y	Pullup	ST/OD
Edge Port (EPORT) (3)						
gint[0]	-	1	I/O	Y	Pullup	ST/OD
gint[1]	-	1	I/O	Y	Pullup	ST/OD
gint2[7]	-	1	I/O	Y	Pullup	ST/OD
USB2.0(2)						
dp	-	1	I/O	N	-	-

Name[1]	Alternate	Qty.	Dir.	Input Sync.[2]	Pull[3,4]	Output Drive (ST/OD/SP)[5]
dm	-	1	I/O	N	-	-
Power Supply(7)						
VCCQ	-	1	-	-	-	-
VDD	-	1	-	-	-	-
VDD5V	-	1	-	-	-	-
VSS	-	1	-	-	-	-
VCCA1	-	1	-	-	-	-
VDDA	-	1	-	-	-	
VDD1P8V	-	1	-	-	-	-

NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. Synchronized input used only if signal configured as a digital I/O.
3. All pullups are disconnected when the signal is programmed as an output.
4. All Not-Single-Chip I/O pins will be put into input mode and be connected to pullups.
5. Output driver type: ST = standard, SP = special, OD = standard driver with open-drain pulldown option selected.

2.4 Signal Descriptions

This subsection provides a brief description of the signals. For more detailed information, reference the specific module section.

2.4.1 Reset Signals

These signals are used to either reset the chip or as a reset indication.

2.4.1.1 Power-On Reset In ($\overline{por}$)

This active-low input signal is used as the external power-on reset. Power-on reset places the CPU in supervisor mode with default settings for all register bits.

2.4.1.2 Reset Out ($\overline{rstout}$)

This active-low output signal is an indication that the internal reset controller has reset the chip.

2.4.2 Clock Signals

These signals are used to support the on-chip clock generation circuitry.

2.4.2.1 Oscillator Pad input (extal)

The signal is the input of Oscillator Pad.

2.4.2.2 Oscillator Pad ouput (xtal)

The signal is the output Oscillator pad .

2.4.2.3 Clock Out (clkout)

This output signal reflects the internal system clock.

2.4.3 Edge Port Signals

2.4.3.1 gint

These bidirectional signals function as either external interrupt sources or GPIO.

2.4.4 USB

These signals are used by the USB module.

2.4.4.1 dp

USB D+ signal pin.

2.4.4.2 dm

USB D- signal pin.

2.4.5 IIC

These signals are used by the IIC module.

2.4.5.1 scl

It is IIC controller bidirection clock pin. It is driven by the host mainly in the communication. Also, the device can drive it low when busy.

2.4.5.2 sda

It is IIC controller bidirection data pin. It is driven by the host in the start/end communication. It is driven by the transmitter when sending data and driven by the receiver when sending acknowlege bit.

2.4.6 USI Signals(USI1/2/3)

2.4.6.1 Smart Card Data Input/Output (isodat)

This signal is used for Smart Card Interface data input/output.

2.4.6.2 Smart Card Clock Signal (isoclk)

This signal is used for Smart Card clock signal.

2.4.6.3 Smart Card Reset Signal (isorst)

This signal is used for Smart Card reset signal.

2.4.7 Serial Peripheral Interface Module(SPI1/2)

These signals are used by the SPI modules and may also be configured to be discrete I/O signals.

2.4.7.1 Master Out/Slave In (mosi1)

This signal is the serial data output from the SPI in master mode and the serial data input in slave mode.

2.4.7.2 Master In/Slave Out (miso1)

This signal is the serial data input to the SPI in master mode and the serial data output in slave mode.

2.4.7.3 Serial Clock (sck1)

The serial clock synchronizes data transmissions between master and slave devices. SCK is an output if the SPI is configured as a master. sck1 is an input if the SPI is configured as a slave.

2.4.7.4 Slave Select ($\overline{ss1}$)

This I/O signal is the peripheral chip select signal in master mode and is an active-low slave select in slave mode.

2.4.8 Power Control

2.4.9 Power and Ground Signals

These signals provide system power and ground to the chip. Multiple signals are provided for adequate current capability. All power supply signals must have adequate bypass capacitance for high-frequency noise suppression.

2.4.9.1 VDD5V

1.8V~5V main power

2.4.9.2 VCCQ

io and analog power.

2.4.9.3 VDD

always on core power

2.4.9.4 VSS

core GND

2.4.9.5 VCCA1

usb phy analog power

2.4.9.6 VDDA

usb phy core power

2.4.9.7 AGND1

usb GND

2.4.9.8 VDD1P8V

Flash power

Section 3 System Memory Map

3.1 Introduction

The address map, shown in **3.2**, includes:

- 16K Bytes of internal read only memory
- 32K Bytes of internal static random-access memory (SRAM)
- 256K Bytes Embedded Flash
- Internal memory mapped registers

3.2 Address Map

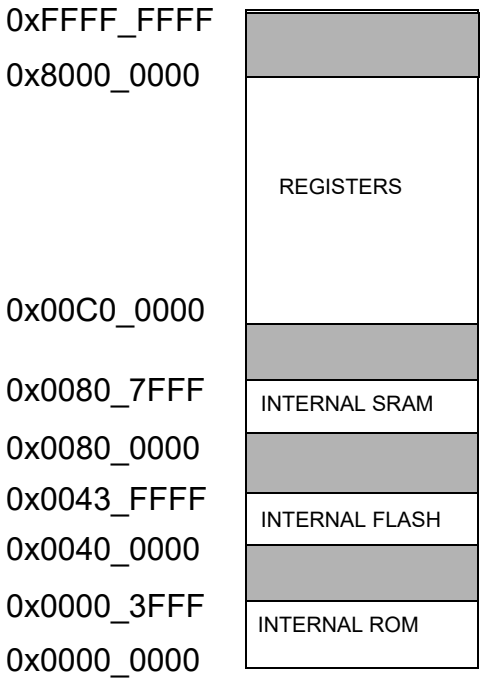


Figure 3-1 Chip Address Map

Table 3-1 Register Address Location Map[1]

Address	Maximum Size	Usage
0x63f0_0000	16Kbyte	IO Control
0x63f0_4000	16Kbyte	Chip configuration (CCM)
0x63f0_8000	16Kbyte	Reset (RESET)
0x63f2_0000	16Kbyte	RSA
0x63f2_4000	16Kbyte	EDMAC0
0x63f3_8000	16Kbyte	LD
0x63f3_c000	16Kbyte	TRNG
0x63f5_c000	16Kbyte	PGD
0x63f6_0000	16Kbyte	SEC_DET
0x63f6_4000	16Kbyte	SHA
0x63f7_0000	16Kbyte	LED
0x63f8_0000	16Kbyte	EFM
0x63f8_8000	16Kbyte	CPM
0x7000_0000	16Kbyte	SPI1
0x7001_0000	64Kbyte	SPI2
0x7003_0000	16Kbyte	SCI1
0x7005_0000	16Kbyte	PIT
0x7006_0000	16Kbyte	PIT32
0x7007_0000	16Kbyte	TC
0x7008_0000	16Kbyte	EPORT1
0x7009_0000	16Kbyte	WDT
0x700b_0000	64Kbyte	I2C
0x700c_0000	16Kbyte	USI1
0x700d_0000	16Kbyte	USI2
0x700e_0000	16Kbyte	USI3
0x700f_0000	16Kbyte	EDMAC1
0x7010_0000	16Kbyte	EPORT2
0x7800_0000	16Kbyte	CRC0
0x7c00_0000	16Kbyte	CRC1
0x0300_0000	16Kbyte	DMAC
0x0100_0000	16Kbyte	USBC
0xfff0_0000	64Kbyte	CACHE
0x00c9_0000	16Kbyte	DES
0x00c9_8000	16Kbyte	ZUC
0x00cf_0000	16Kbyte	AES
0x00de_0000	64Kbyte	SMS4

NOTES:

1. See module sections for details of how much of each block is being decoded. Accesses to addresses outside the module memory maps(and also the reserved area) will not be responded to and will result in error exception.

System Memory Map

Appendix A Preliminary Electrical Characteristic

A.1 General

This section provides electrical parametrics and electrical ratings for the microcontroller unit.

A.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the Chip can be exposed without permanently damaging it. See **Table A-1** , **Table A-2** and **Table A-3**

The Chip contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings. Refer to **Table A-4**,**Table A-5** and **Table A-6** for guaranteed operating conditions.

Table A-1 Absolute Maximum Ratings(Commercial Application)

Num	Rating	Symbol	Value	Unit
1	Operating temperature range	T_{OPT}	0 to +70	^{O}C
2	Storage temperature range	T_{STG}	-40 to +125	^{O}C

Table A-2 Absolute Maximum Ratings(Industrial Application)

Num	Rating	Symbol	Value	Unit
1	Operating temperature range	T_{OPT}	-40 to +85	^{O}C
2	Storage temperature range	T_{STG}	-40 to +125	^{O}C

Table A-3 Absolute Maximum Ratings(Automotive Application,AEC-Q100 qualified)

Num	Rating	Symbol	Value	Unit
1	Operating temperature range	T_{OPT}	-40 to +105	^{O}C
2	Storage temperature range	T_{STG}	-40 to +125	^{O}C

A.3 Electrostatic Discharge (ESD) Protection

Table A-4 ESD Protection Characteristics

Parameter[1,2,3,4,5]	Symbol	Value	Units	Reference Standard
ESD target for human body model	HBM	3500	V	ANSI/ESDA/JEDEC JS-001-2014
ESD charge device model	CDM	500	V	JEDEC EIA/ JESD22-C101F
Latch Up	Latch UP	200	mA	JEDEC STANDARD NO.78D NOVEMBER 2011

NOTES:

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

A.4 DC Electrical Specifications

Table A-5 DC Electrical Specificatios(IO 1.8V)

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{DDH}	1.62	1.8	1.98	V
Input High Voltage	V_{IH}	$0.7*V_{DDH}$	—	V_{DDH}	V
Input Low Voltage	V_{IL}	0	—	$0.3*V_{DDH}$	V
Output High Voltage	V_{OH}	$0.8*V_{DDH}$	—	V_{DDH}	V
Output Low Voltage	V_{OL}	0	—	$0.2*V_{DDH}$	V
Input Leakage Current	I_{IN}	—	—	1	uA
Input Pull-up Resistor	R_{PU}	—	—	32.4	kΩ
Input Pull-down Resistor	R_{PD}	—	—	32.4	kΩ

Table A-6 DC Electrical Specificatios(IO 3.3V)

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{DDH}	2.97	3.3	3.63	V
Input High Voltage	V_{IH}	2	—	V_{DDH}	V
Input Low Voltage	V_{IL}	0	—	0.8	V
Output High Voltage	V_{OH}	2.4	—	V_{DDH}	V
Output Low Voltage	V_{OL}	0	—	0.4	V
Input Leakage Current	I_{IN}	—	—	1	uA
Input Pull-up Resistor	R_{PU}	—	—	19.4	kΩ
Input Pull-down Resistor	R_{PD}	—	—	16	kΩ

[redacted]

Appendix B Production Parameters

B.1 General

This section provides parameters for below items:

- Package Outline Dimension (POD) of package SSOP28
- Package Outline Dimension (POD) of package QFP48_R
- Package Outline Dimension (POD) of package QFN48_N
- Package Outline Dimension (POD) of package QFN32

B.2 POD of Package

Figure B-1 POD of package SSOP28

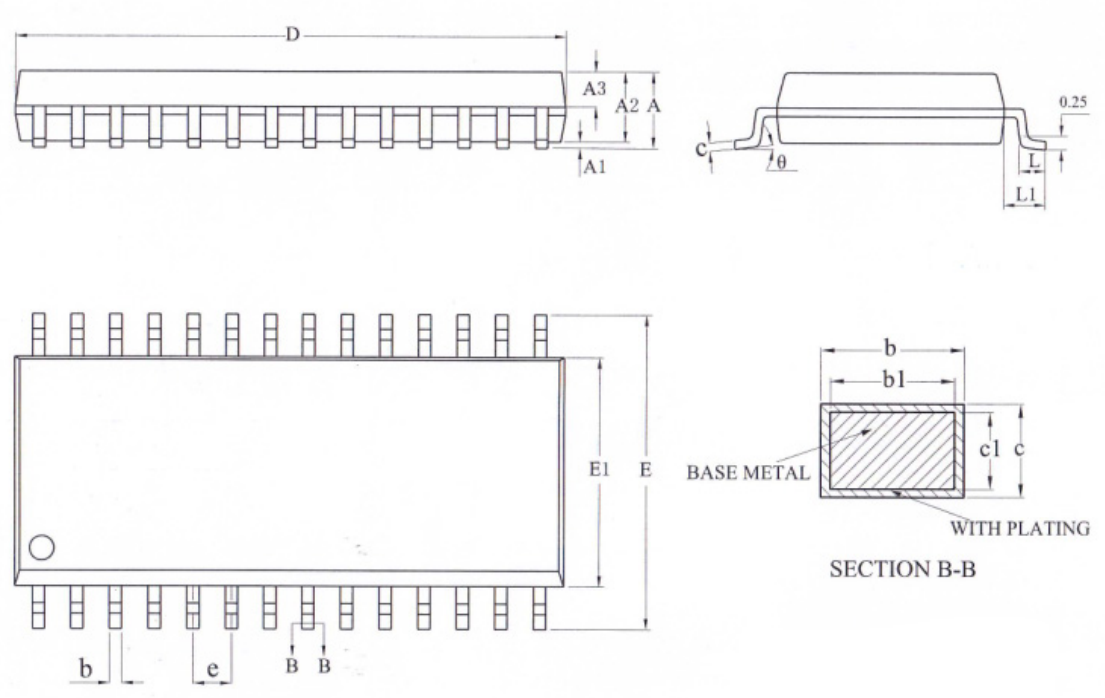


Table B-1 POD Parameters of package SSOP28

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	2.00
A1	0.05	-	0.25
A2	1.65	1.75	1.85
A3	0.75	0.80	0.85
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.15	-	0.19
c1	0.14	0.15	0.16
D	10.10	10.20	10.30
E	7.60	7.80	8.00
E1	5.20	5.30	5.40
e	0.65BSC		
L	0.75	-	1.05
L1	1.25REF		
θ	0^o		8^o

B.3 POD of Package QFP48_R

Figure B-2 POD of package QFP48_R

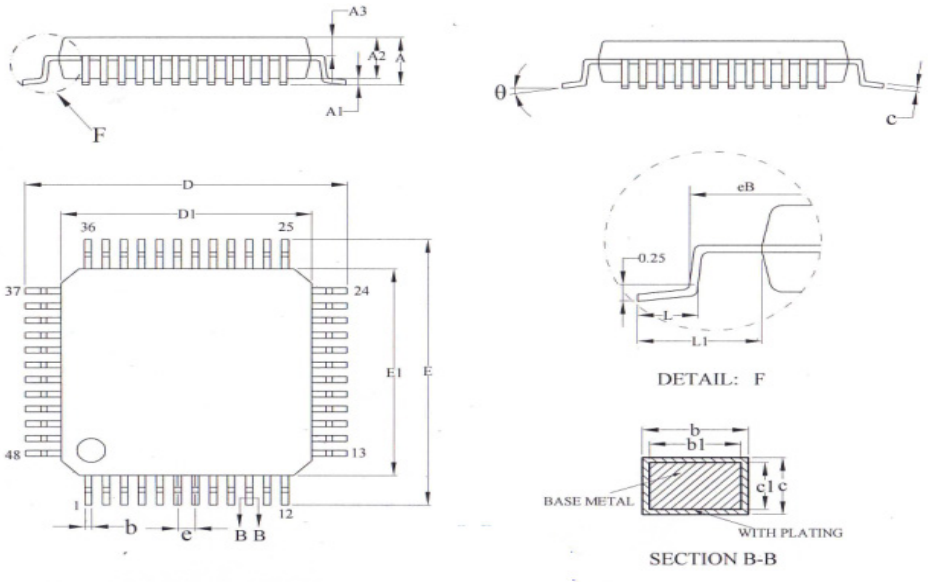


Table B-2 POD Parameters of package QFP48_R

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.40	-	0.65
L1	1.00REF		
θ	0^o	-	7^o

B.4 POD of Package QFN48_N

Figure B-3 POD of package QFN48_N

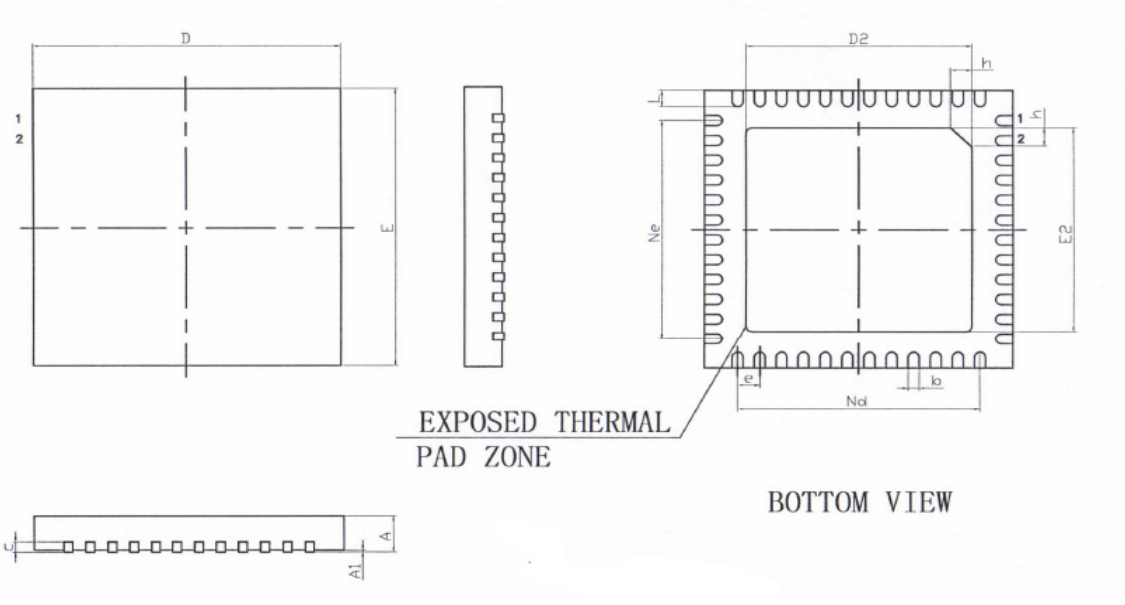


Table B-3 POD Parameters of package QFN48_N

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F dimension	177*177		

B.5 POD of Package QFN32

Figure B-4 POD of package QFN32

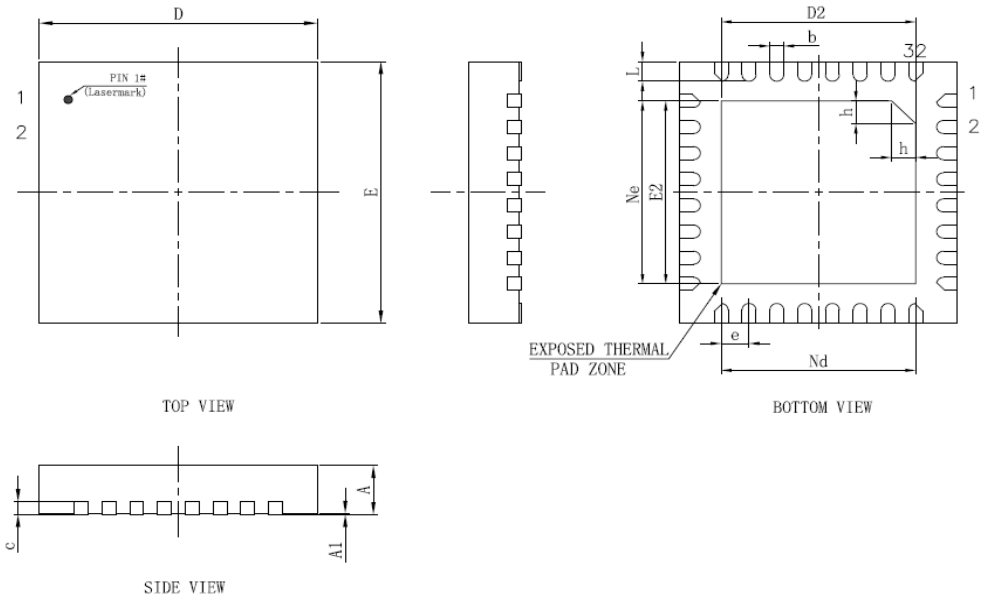


Table B-4 POD Parameters of package QFN32

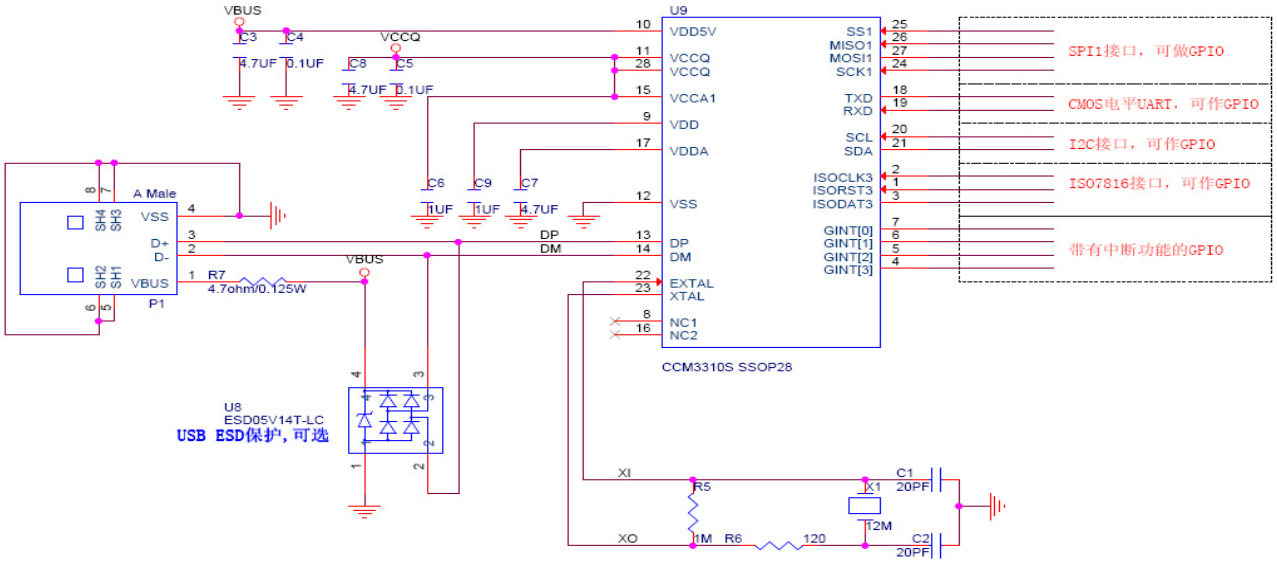
SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F dimension	122*122		

[redacted]

Appendix C Circuit principium

C.1 Referenced Design Diagram

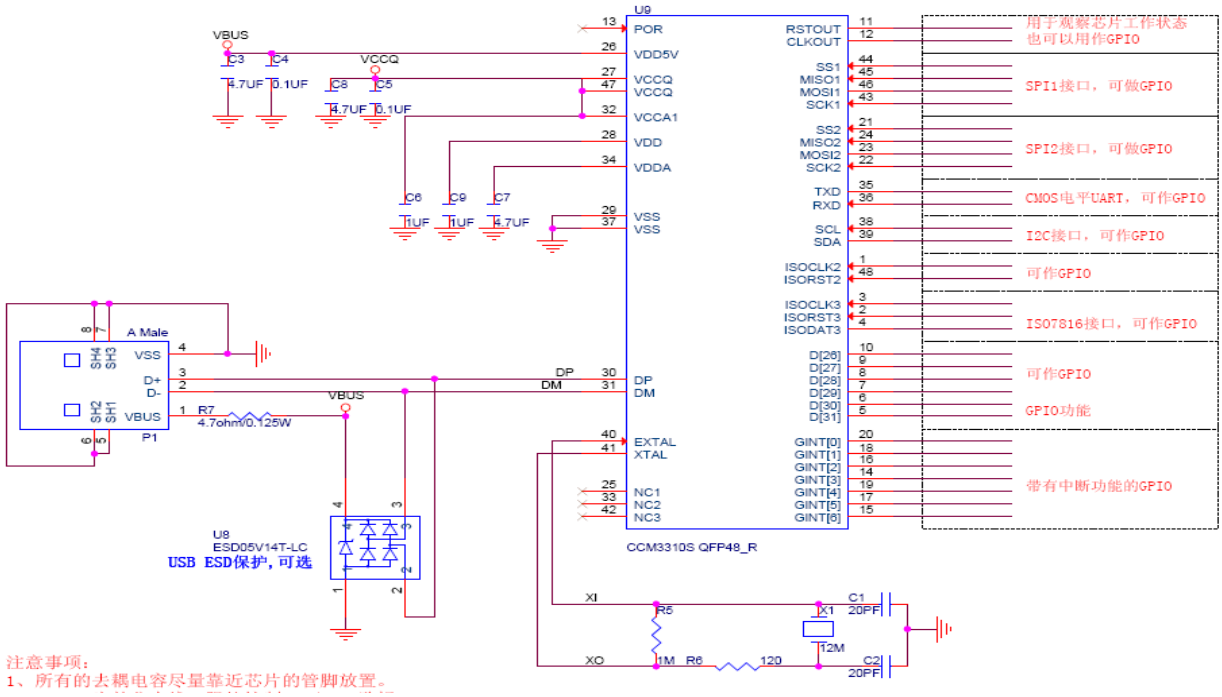
Figure C-1 SSOP28 Referenced Design Diagram



C.2 Notice

- The power without capacity need close to pin set.
- dp dm is differential signal line, the impedance controal at 90+/-10%.
- the suported capacitor is X7R,endurance is above 10V.
- I2C pad is configed as OD gate. need to connect to pullup resistors.
- Resistor R7 is 0603 package, to match power request.

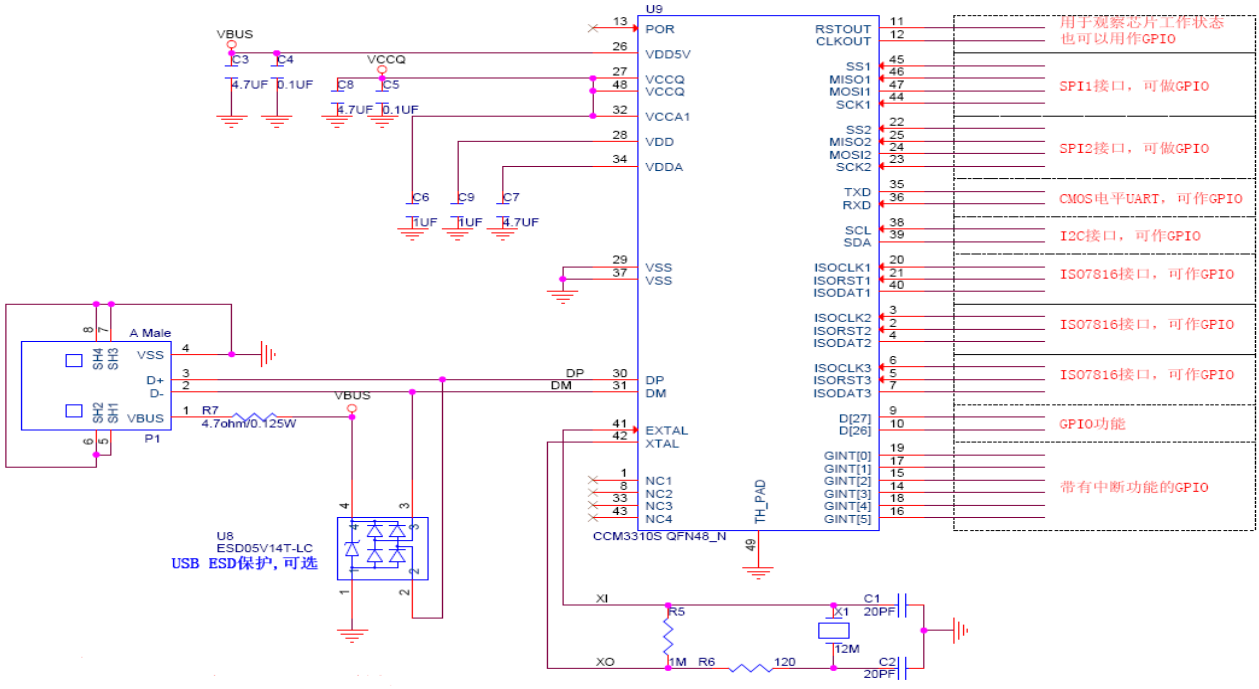
Figure C-2 QFP48_R Referenced Design Diagram



C.3 Notice

- The power without capacity need close to pin set.
- dp dm is differential signal line, the impedance controal at 90+/-10%.
- the suported capacitor is X7R,endurance is above 10V.
- I2C pad is configed as OD gate. need to connect to pullup resistors.
- Resistor R7 is 0603 package, to match power request.

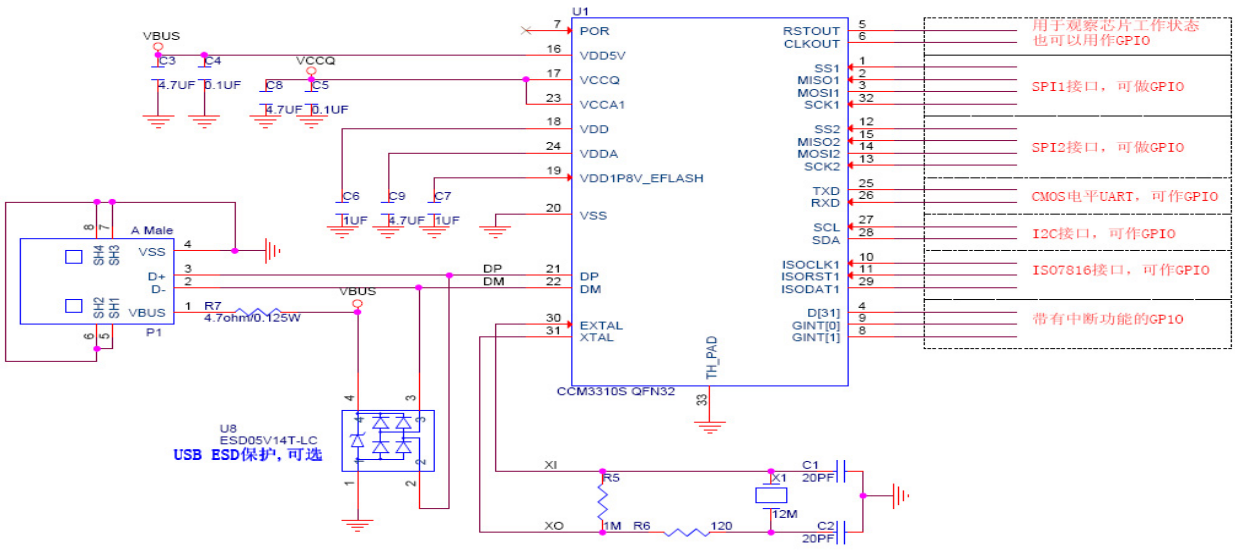
Figure C-3 QFN48_N Referenced Design Diagram



C.4 Notice

- The power without capacity need close to pin set.
- dp dm is differential signal line, the impedance controal at 90+/-10%.
- the suported capacitor is X7R,endurance is above 10V.
- I2C pad is configed as OD gate. need to connect to pullup resistors.
- Resistor R7 is 0603 package, to match power request.

Figure C-4 QFN32 Referenced Design Diagram



C.5 Notice

- The power without capacity need close to pin set.
- dp dm is differential signal line, the impedance controal at 90+/-10%.
- the suported capacitor is X7R,endurance is above 10V.
- I2C pad is configed as OD gate. need to connect to pullup resistors.
- Resistor R7 is 0603 package, to match power request.